“Future HDI”
An HDPUG project Proposal

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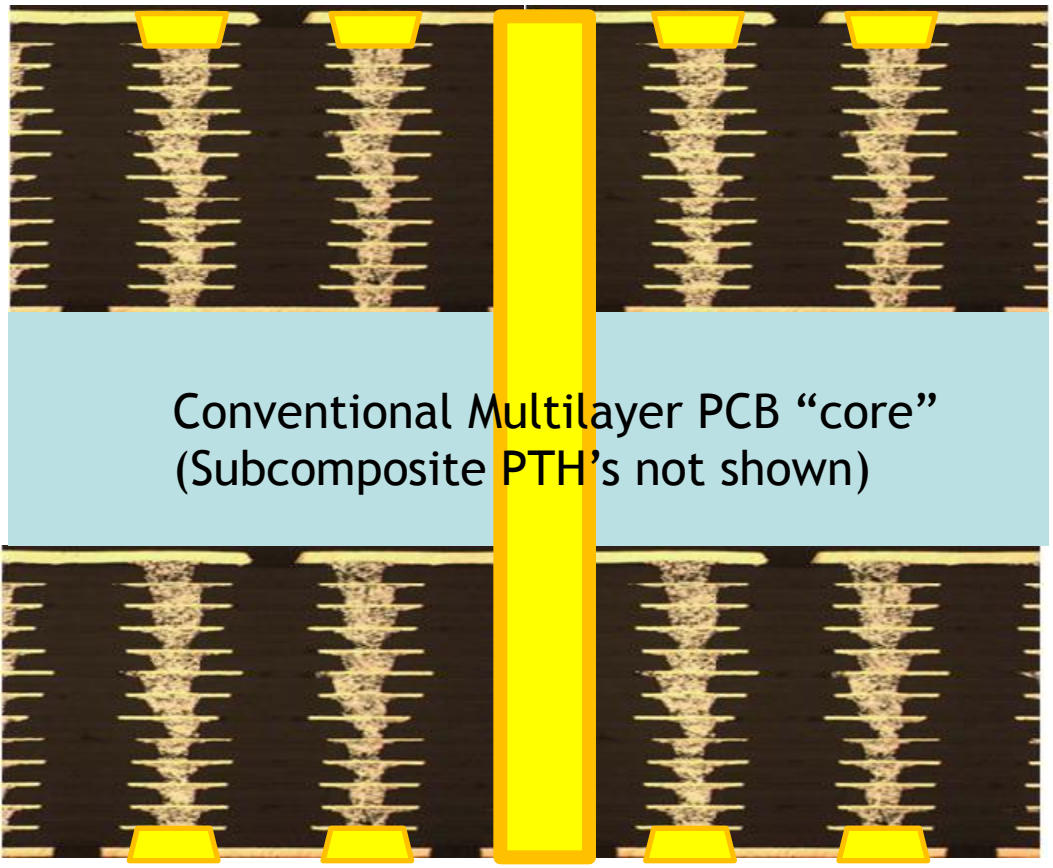
Background

- BGA pitch is moving steadily downward.
- High I/O BGAs are common at 1mm and 0.8mm pitch today and starting to appear at 0.65mm pitch.
- Consumer PCB's (smart phone, tablet, etc.) have already moved to large I/O BGA's at 0.5 and even 0.4mm pitch.
  - Example: TI OMAP4 processor 500+ I/O at 0.4mm pitch
  - This is supported by Any Layer/Every Layer HDI PCB's that are very thin (typically 0.8mm thick or less)
    - Too thin for Telecom/Server applications
    - Reliability questions
  - These types of packages require 3 + stacks and growing of microvias for routing (depending on how many I/O and design specifics) just to escape route these packages.
- It is inevitable that High I/O BGAs for High complexity products (Telecom, Server, etc.) will also trend downward in pitch, following the consumer trend.

Background (2)

- 0.65mm pitch is the practical limit for through hole vias in volume production with high reliability and even this has many design and fabrication challenges.
- The standard consumer “Any Layer” via technology is not directly compatible with large complex boards used in these high reliability industries
- Current sequential lamination technologies are too expensive to support future needs.
  - Also, ALV is better aligned with high speed & high density requirements
- A new construction concept is proposed merging aspects of today’s high end designs with aspects of consumer PCB’s to tackle these challenges.
  - This concept needs confirmation and validation to make it a reality
  - Reliability and design limitations need to be established.

The Concept



Not to scale – thickness of the top and bottom stack is much thinner than the core

“Any layer” outer sub “stack” construction (Sintered Cu paste)

L1-2 and N to N-1 Cu Plated – not sintered paste

Includes Cu PTH

Any layer stack – very thin (like a typical consumer technology) - 0.8mm thick or less. Total board thickness 2.4 mm or greater. No plating/thin Cu supports fine trace and spacing

Bottom “stack” optional – may only require single side.

Maximum of 4 laminations, 2 (3 with VIPPO) plating steps

No stacking of Any layers on sub composite buried via? (to simplify construction and eliminate a major reliability concern)

Additional

- The HDI “stack” is current consumer technology.
- The sub composite core is standard technology.
- Connection of the HDI “stack” to the sub composite core “should” be only an extension of the same Cu sintered paste technology (some limited development required)
- There are other issues that need to be answered to be able to apply this to real high reliability products

Reliability Questions to Evaluate

- Current carrying
  - What is the maximum current a single stack of sintered Cu paste vias (or other proposed technology) can support?
    - Stack height/via size function
- IST/Thermal cycle reliability
  - What is the Pb-free survivability and IST thermal cycle reliability of a stack of microvias (10 layers?) in a thick composite board as shown?
- CAF
  - Are the sintered Cu paste vias susceptible to CAF?
    - If so – at what dimensions?
- Component interaction reliability – Example – Large CBGA or similar
  - Will the shear stresses of large high strain packages cause failures in the HDI stack of vias in ATC, or reflow cool down (as was seen for early large silicon on ALIVH BGA substrates)?

Reliability Questions to Evaluate (2)

- Material Stability
  - How stable is the sintered Cu paste material vs plated Cu?
    - Thermal aging
    - Humidity
- Electrical performance
  - Related to material stability, what is the electrical performance of series of sintered Cu paste vias?
    - Impedance coupons with vias

Project Proposal

- Design a test vehicle to answer the questions and serve as a development platform for PCB fabricators.
  - Include 10 layer stack HDI Via Arrays at 0.5mm, 0.4mm, and 0.3mm pitch for CAF testing. (Note 0.3 mm may not really be practical at this time – but in the proposal if we can support it)
  - Include IST coupons for IST and delam testing
  - Include a high strain component (proposal – the previously tested 483 CBGA) to evaluate effect of very high strain package on HDI stack via survivability in ATC. 1 per board
  - Include design features to test current carrying capacity limits of the 10 stack HDI structure.
  - Include Impedance coupon(s) with sintered Cu paste vias

Project Proposal (2)

- Fabricate PCBs at multiple fabricators. They choose the method and materials.
  - Propose minimum of 8 PCB's from each of at least 4 fabricators
- Assemble 32 boards (8 each from 4 fabricators)
- CAF Testing of the HDI via arrays – after reflow only (separable after assembly)
- IST and Delam testing (using IST tester to simulate reflow) – as built coupons (separable before assembly)
  - Includes stabilization/characterization capabilities
- ATC Testing and FA of the High Strain component – FA only to check for via failures.
- TDR testing before and after thermal aging, humidity
- Evaluate results and establish basic design rules.
- Final Report

Project Actions

- Define/Design Test Vehicle (TBD), 5 sections
  - IST – PWB interconnect
  - CAF – via arrays similar to MRT – but at pitches of 0.5, 0.4, and 0.3mm, in the “any layer stack” section only.
  - ATC section – daisy chain component – identify and purchase
  - Current carrying evaluation – 10 stack – how to test?
  - Impedance coupon(s)
- Fabricate Test vehicles (multiple fabricators)
- Assemble Test Vehicle (EMS - TBD) – separate for tests
  - ATC – Alcatel-Lucent
  - IST – PWB Interconnect
  - Current carrying evaluation, Impedance testing – TBD
  - CAF Test – TBD
  - FA – TBD
- Evaluate results – define basic design rules (Fabricators)
- Final report – Team