Electro-Chemical Migration

Going to Implementation Stage

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HDP User Group Member Meeting

Host: Flextronics

Santa Clara, CA

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Problem Statement

The current industry standard test protocols for Bare Boards and Board Assemblies were originally developed to identify highly ionic contaminant levels (halides) after a cleaning process. These test protocols are not completely effective at identifying ECM exposures from no-clean flux residues.

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Background

1. Various forms of corrosion and Electro Chemical Migration failures on products that pass the current cleanliness and corrosion resistance test protocols have demonstrated that these test procedures are not effective.

2. The failure mechanism is the same regardless what segment of the electronics industry the PCBA is used.

3. The current testing does not take into consideration various acceleration factors associated with no clean flux and product design features.

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Project Goal

Identify required enhancements to the current industry specifications, test methods, and coupon design to mitigate the electro-chemical migration and corrosion induced failures when no clean flux systems are used.

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Project Scope

Areas to investigate:

- Cleanliness testing
- Corrosion resistance testing
- ECM testing
- Maximum acceptable residue levels
- Influence of PCB manufacturing defects
- Influence of PCBA design features

Areas not to be investigated:

- Conformal coating over no-clean fluxes. This may allow ECM under the conformal coating.
- Solder mask test standards for ECM controls.
- ImAg creep corrosion (covered by multiple current projects)

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Project Deliverables

1. Propose changes to:
    - The Standards
    - Test Methods
    - Test Coupons

   for the IPC Committee on Coatings & Cleanings.

2. Write a white paper and/or article.

3. Internal report for Membership.

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Project Flow Plan

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Ø1
Verification Phase (Product)

Existing product used

↓

Modified SM

↓

Assemble Bds.

↓

ATC Testing

↓

Verify corrosion Reproducibility

Completed By Vendor

Ø2
Correlation Phase (IPC B-52)

Modify B-52 Artwork

↓

Fabricate Boards

↓

Cleanliness CK.

↓

Assemble Bds.

↓

ATC Test

↓

Failure Analysis

↓

Complete Full Variables criteria

Ø3
Full Variables Phase (IPC B-52?)

Select Test Vehicle

↓

Fabricate Boards

↓

Cleanliness CK..

↓

Assemble Bds.

↓

ATC Test

↓

Failure Analysis

↓

Write Report and spec changes

Phase 1 (Completed)

Ø1
Verification Phase (Product)

Existing product used

↓

Modified SM

↓

Assemble Bds.

↓

ATC Testing

↓

Verify corrosion Reproducibility

Completed By Vendor

Purpose:

1. To insure that we can reproduce the failure in real time.

Deliverables:

1. A methodology to recreate the failure mechanism for the project

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Phase 1 (Completed)

- Open Trace DOE

	PCB Trace Location	WK#6/17(First Week)	WK#7/1	WK#7/15	WK#7/29	WK#8/12
3 Volts	PS_ON Before SMT					
	PS_ON After WS					
No Voltage	SUSCLK Before SMT					
	SUSCLK After WS					

Phase 2 (Starting Now)

Ø2
Correlation Phase (IPC B-52)

Modify B-52 Artwork
↓
Fabricate Boards
↓
Cleanliness CK.
↓
Assemble Bds.
↓
ATC Test
↓
Failure Analysis
↓
Complete Full Variables criteria

Purpose:

1. To insure that we can induce the failures in the IPC TV
2. Test measurement of Variables before doing full DOE.

Deliverables:

1. Verification of DOE.
2. Confidence in the modified B52 TV.
3. Direction of IPC Standards change.

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Modify B-52 Test Vehicle

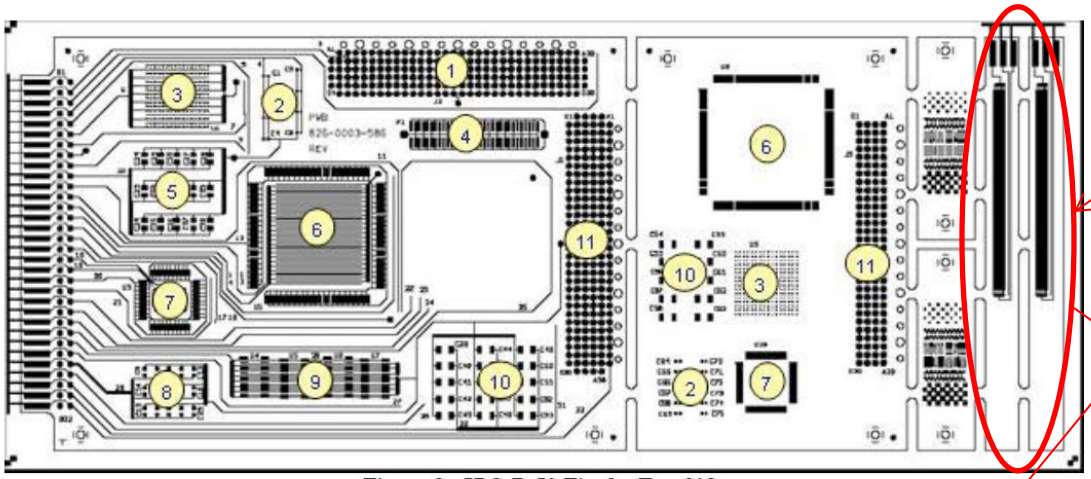

Figure 8 - IPC-B-52 Final – Top Side

Modifications:

1. Reverse the SIR coupons from Top side to Bottom side.
2. Add Perpendicular Solder Mask slots for potential ECM.
3. Add voltage connections to 0805 sites.

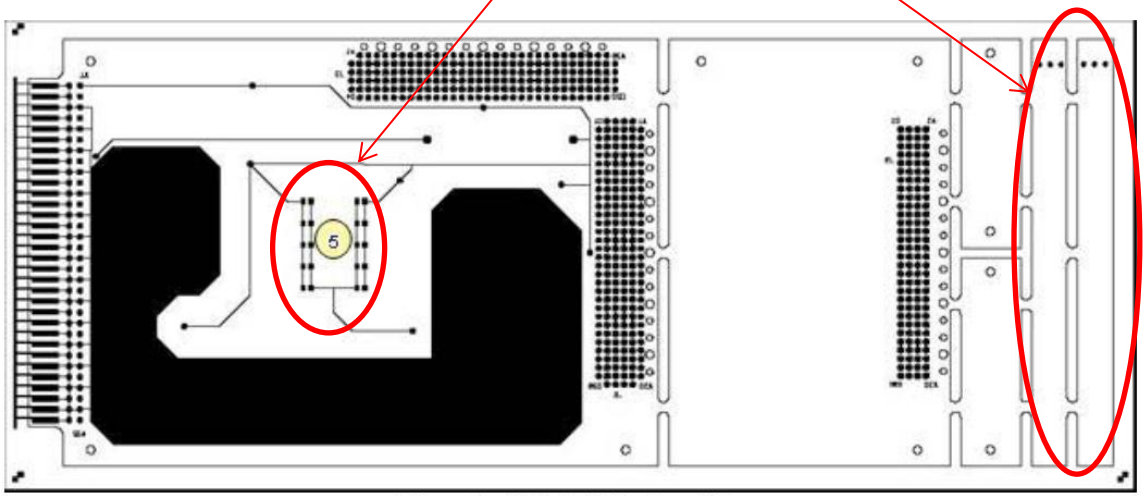

Figure 9 - IPC-B-52 Bottom Side

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DOE Test Matrix

- Flux application – 2 levels (high, low)
- Flux type – 2 levels (high rosin, low rosin)
- Voltage Bias – 3 levels (0, 3, 10)
- Replicates in DOE – 2

Custom Design

Design	Custom Design
Criterion	D Optimal

Screening
Model
DOE Dialog

Columns (7/0)
Flux Type ✱
Voltage ✱
Flux Applied ✱
Ground Pad Corrosion ✱
Voltage Pad Corrosion ✱
Ground trace SM open corrosion ✱
Voltage trace SM open corrosion ✱

Rows

All rows	24
Selected	0
Excluded	0
Hidden	0
Labelled	0

	Flux Type	Voltage	Flux Applied	Ground Pad Corrosion	Voltage Pad Corrosion	Ground trace SM open corrosion	Voltage trace SM open corrosion
1	High Rosin (Alpha EF-8000)	10	High	•	•	•	•
2	High Rosin (Alpha EF-8000)	3	High	•	•	•	•
3	High Rosin (Alpha EF-8000)	3	Low	•	•	•	•
4	High Rosin (Alpha EF-8000)	3	High	•	•	•	•
5	Low Rosin (Alpha EF-6000)	10	Low	•	•	•	•
6	High Rosin (Alpha EF-8000)	10	High	•	•	•	•
7	Low Rosin (Alpha EF-6000)	10	Low	•	•	•	•
8	Low Rosin (Alpha EF-6000)	10	High	•	•	•	•
9	High Rosin (Alpha EF-8000)	3	High	•	•	•	•
10	Low Rosin (Alpha EF-6000)	3	Low	•	•	•	•
11	Low Rosin (Alpha EF-6000)	3	High	•	•	•	•
12	Low Rosin (Alpha EF-6000)	10	High	•	•	•	•
13	High Rosin (Alpha EF-8000)	10	Low	•	•	•	•
14	High Rosin (Alpha EF-8000)	3	Low	•	•	•	•
15	High Rosin (Alpha EF-8000)	10	High	•	•	•	•
16	Low Rosin (Alpha EF-6000)	10	High	•	•	•	•
17	Low Rosin (Alpha EF-6000)	10	Low	•	•	•	•
18	High Rosin (Alpha EF-8000)	3	Low	•	•	•	•
19	Low Rosin (Alpha EF-6000)	3	Low	•	•	•	•
20	Low Rosin (Alpha EF-6000)	3	High	•	•	•	•
21	Low Rosin (Alpha EF-6000)	3	High	•	•	•	•
22	High Rosin (Alpha EF-8000)	10	Low	•	•	•	•
23	High Rosin (Alpha EF-8000)	10	Low	•	•	•	•
24	Low Rosin (Alpha EF-6000)	3	Low	•	•	•	•

The DOE test matrix would require 24 samples for two replicates, plus 12 samples for non-tested controls.

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Liquid Flux Data

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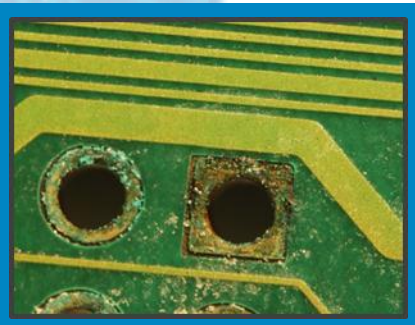
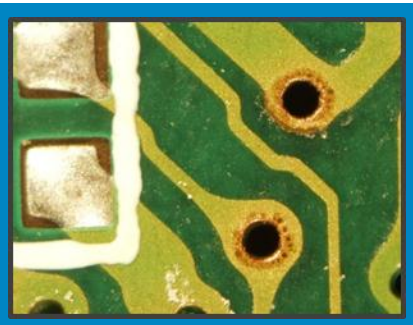
Liquid Wave / Selective Wave Solder Flux								
Supplier		Product Name	Flux Classification	No-Clean	Water Soluble	Classification	Flux Solids	H, M, L
1	Alpha Metals	RF800	ROL0	x		Rosin	4.1	M
		NR330	ORL0	x		VOC Free	4.0	M
		EF3215	ORL0	x		Low VOC	6.2	H
		EF6850HF	ROL0	x		Halogen Free VOC	4.0	M
		EF6000	ORL0	x		Low Solids No-Clean	2.2	L
		EF8000	ROL0	x		Low rosin No-Clean	6.0	L
		EF2202	ORL0	x		Low VOC	3.5	L
		EF-6100P	ORL0	x		VOC	4.3	M
		Lonco 3355-11	ORH1		x	Organic Acid High Activity	17.0	H
		Lonco 3355-HB	ORH1		x	Organic Acid High Activity	30.0	H
		WS362-25	ORM0		x	Organic Acid Med Activity	25.0	H
2	Kester	958M	ROL0	x		VOC	3.6	M
		959T	ORL0	x		VOC	2.9	L
		979	ORL0	x		VOC Free	4.5	M
		2331-ZX	ORH1		x		33	H
		2220-VF	ORH1		x	VOC Free	7.0	H
3	Tamura	ULF210-RN	ROL0?	x		Rosin	5.0	H
4	Senju	1077	ROL1?	x		Rosin?	7.0	H
5	Interflux	IF2005M	ORL0	x		Alcohol Based	1.8	L
		Terrlfic RP 65	ORL0			VOC Free	6.5	H
6	ShenMao	SM-816	ROL0	x		Rosin	3.4	L
7	TongFang	TF-328-2	ROL0?	x		Rosin	2.5	L
8	Vital	GW2021-2	REL0	x		Resin	3.9	M
9	Nihon Superior	NS-850	ROL0	x		Rosin	15.0	H

L	<= 3.5%
M	>3.5%, <5%
H	>5%

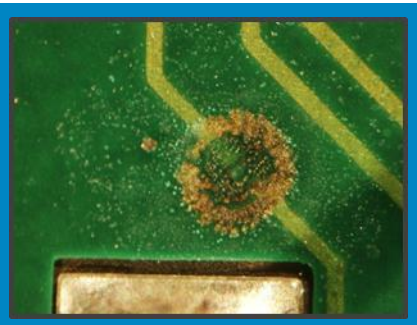
No clean ECM corrosion failures



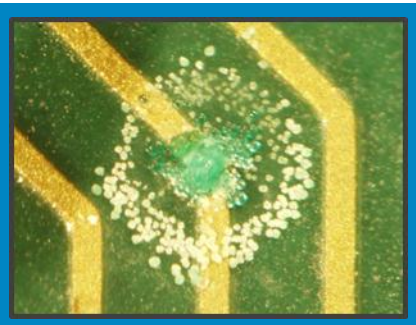
Surface corrosion



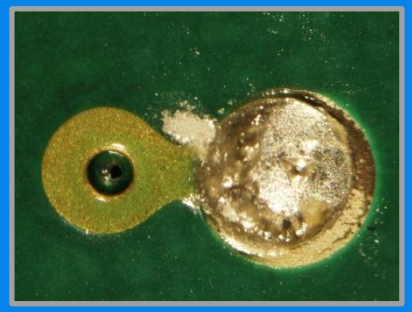
Solder mask Porosity



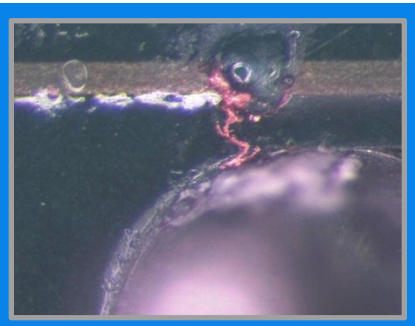
Open trace / solder mask opening



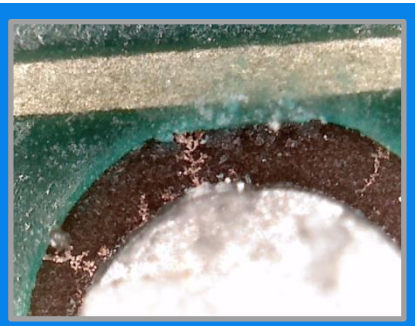
Open trace / solder mask opening



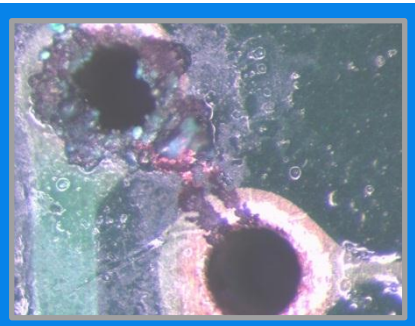
Surface corrosion



Dendrite / short / open



Dendrite / short



Dendrite / short

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Phase 2 Test Plan

- Purpose is to correlate J-STD-004 data with modified B-52 data findings

Test	IPC-TM-650	Test Board / Coupons	Qty /cell	Controls (non tested)	No of Test Cells	Total Processed Boards	Blanks	Total Boards
SIR Test	2.6.3.7	IPC B-24	5	2	4	20	1	29
Copper Mirror Test	2.3.32	Copper Mirror coupon	3	2	4	20	1	21
Corrosion Test	2.6.15	Cu Clad Coupons	3	2	4	20	1	21
ECM Test	2.6.14.1 2.6.3.3	IPC B-25A	5	2	4	28	1	29
DOE Test Vehicle		IPC B-52 modified	24	12	1	36	1	37

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SIR

- Biased ~ IPC B-24
- 40°C/90% RH
- Seven days

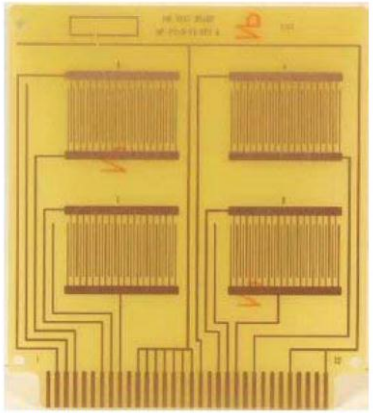


Figure 1. IPC-B-24 Test Vehicle

Figure 3: Flux corrosion of copper conductors.

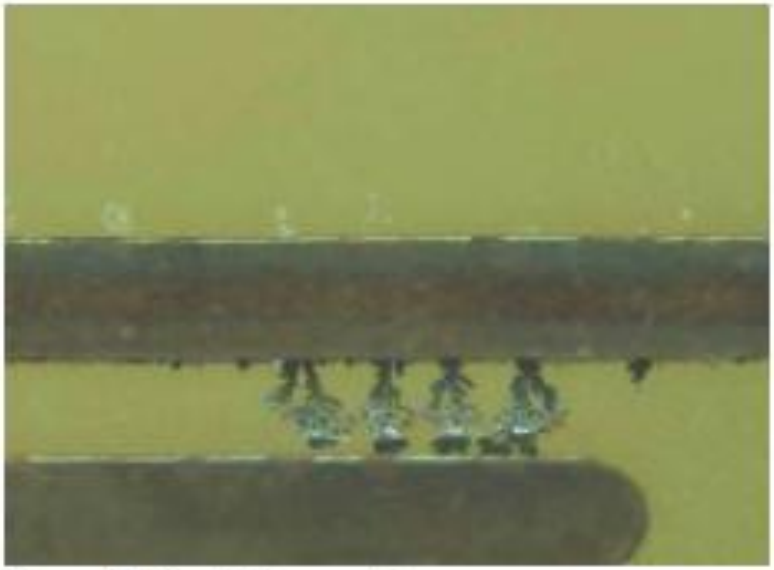
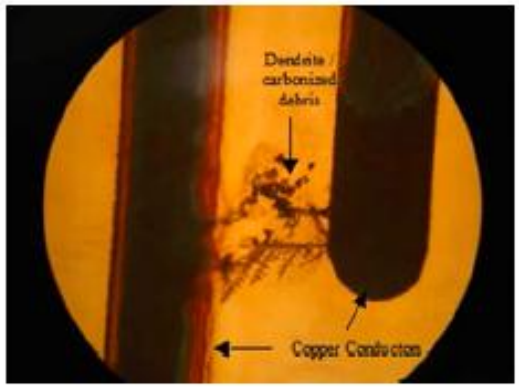
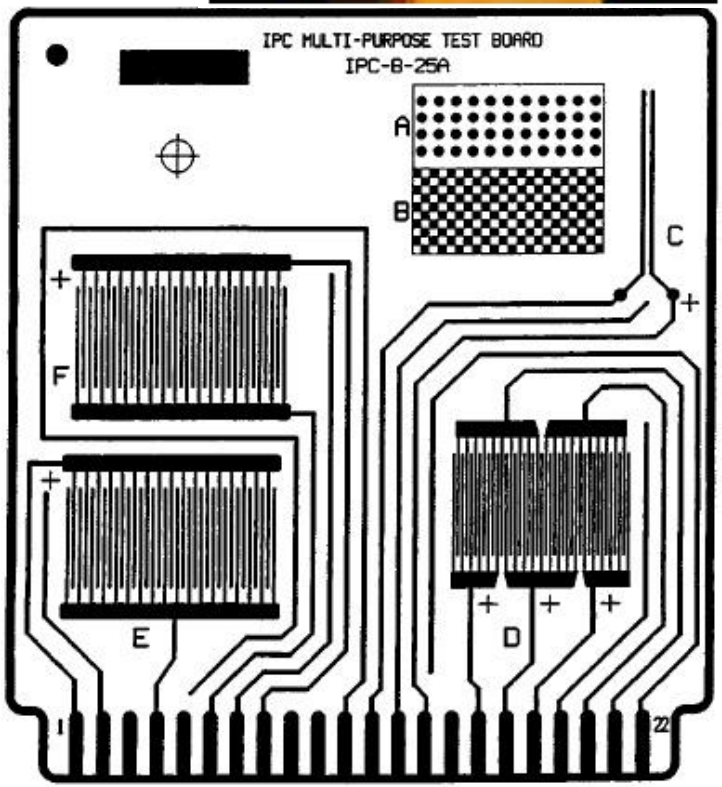


Figure 4: Dendritic growth.

ECM

- IPC B-25A ~ Biased
- 65°C/85% RH
- 21 days
- IR measurement at 96 hours
- 500 hr. measurement
- 1 decade drop in IR constitutes a failure





Copper Mirror

- Flux application as received
- Classify flux corrosivity

Figure 1: Copper mirror test. L = no breakthrough, M = less than 50% breakthrough, H = greater than 50% breakthrough.

Corrosion

- Flux reflowed onto coupon
  - 50°C/95% RH
  - 7 days

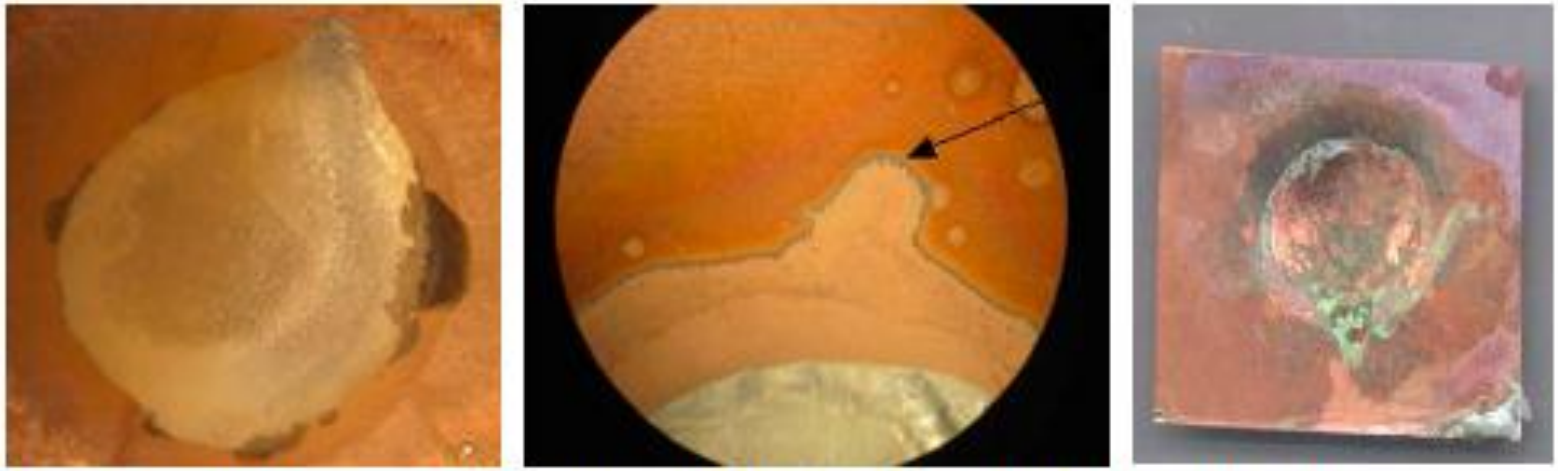


Figure 2: Corrosion test showing (l–r) no corrosion, minor corrosion and major corrosion.

Modify B-52 Test Vehicle

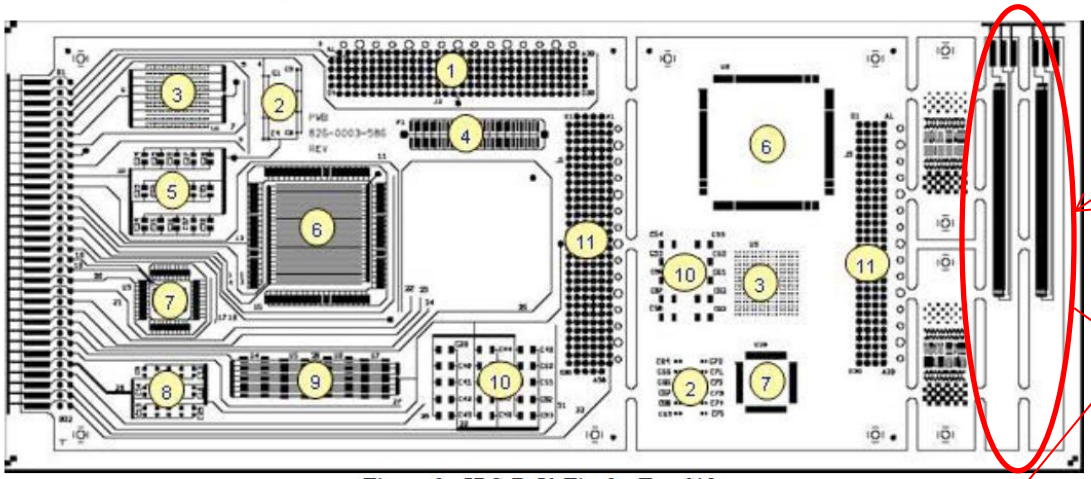


Figure 8 - IPC-B-52 Final – Top Side

Modifications:

1. Reverse the SIR coupons from Top side to Bottom side.
2. Add Perpendicular Solder Mask slots for potential ECM.
3. Add voltage connections to 0805 sites.

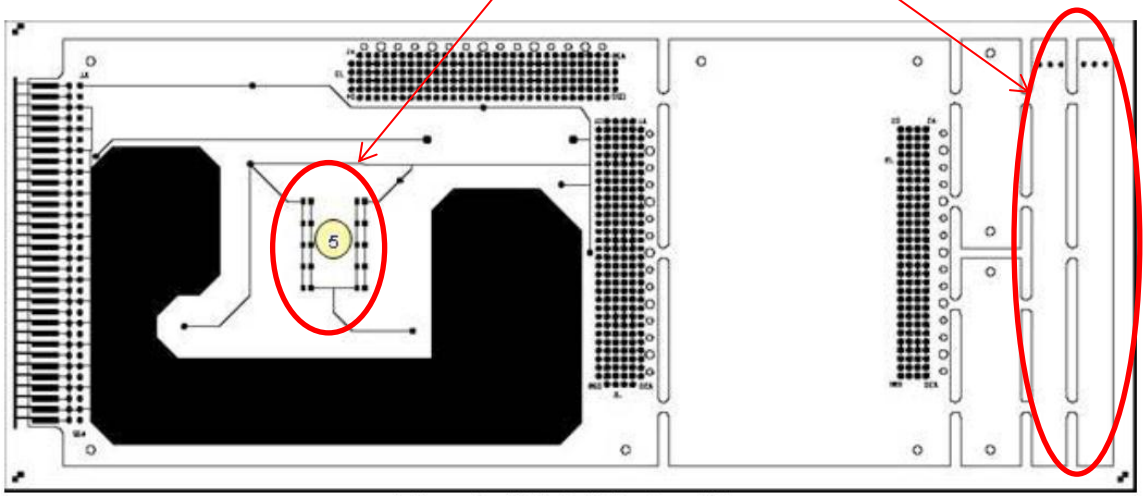


Figure 9 - IPC-B-52 Bottom Side

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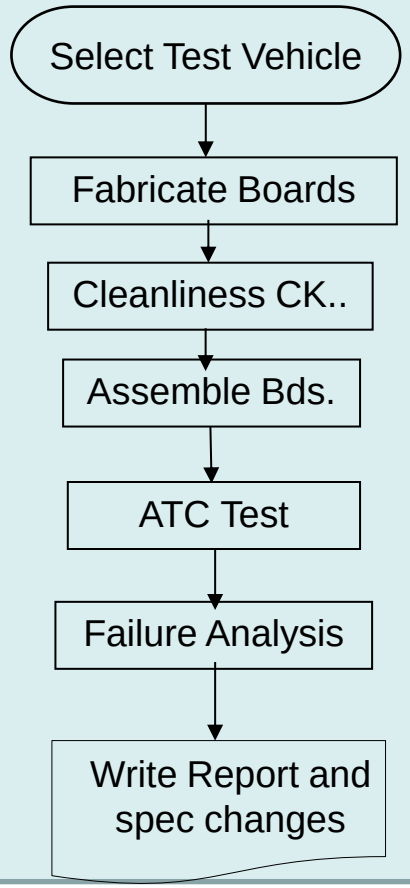
Phase 3

Ø3
Full Variables Phase (IPC B-52?)



Purpose:
Define the process criteria to insure:

1. Board Cleanliness
2. No corrosion resistance
3. No ECM

Deliverables:

1. Propose changes to IPC on Standards, Test Methods, Test Coupons.
2. Write a white paper and/or article.
3. Internal report for Membership.

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Project Schedule - Ø2

ACTIVITY	Company	Est.Date	Actual
• Provide Gerber for latest IPC B-52 Bd.	Plexus	Comp	Comp
• Provide Modify instructions to TTM	Dell	Comp	Comp
• Modify test board designs	TTM	03/07/14	
• Ship Fab test boards	TTM	03/21/14	
• Serialize boards	Kyzen	03/28/14	
• Cleanliness characterization of PCB's	Kyzen	04/11/14	
• Ship wave solder fluxes to Plexus	Enthone	04/11/14	
• Ship Assembly TV (Apply Fluxes,)	Plexus	05/09/14	
• Perform ATC type testing on boards	Agilent	10/24/14	
• Perform SIR type testing on boards	Dell	11/07/14	
• Define post-test analysis plan	Kyzen	11/03/14	
• Perform post-test analysis	Dell	11/21/14	
• Perform post-test analysis	Foresite	12/05/14	
• Write Report	Kyzen	01/23/15	

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- Agilent
- Alcatel-Lucent
- Arlon
- Celestica
- Ciena
- Cisco
- Dell
- Enthone
- Ericsson
- Flextronics
- Fujitsu
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