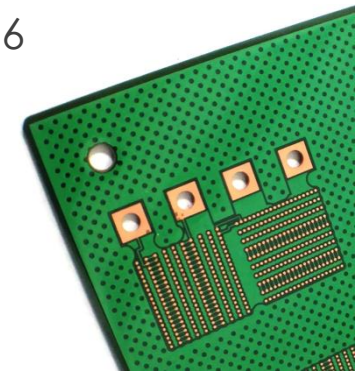
Ultra Thin HDI Multi-purpose Test Vehicle

Idea Stage Project
C.B. Katzko, TTM Technologies

HDPUG Member Meeting, 2014 February 26
Santa Clara, California, USA



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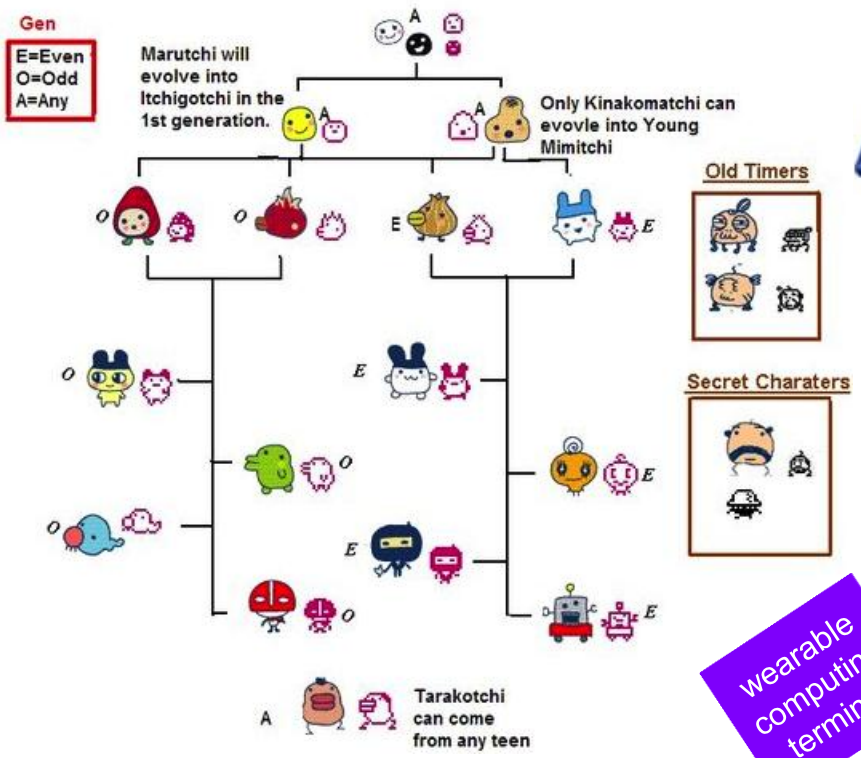
Disclaimer

"Only a few Tamagotchi were harmed in preparation of this presentation"



wearable computing terminal

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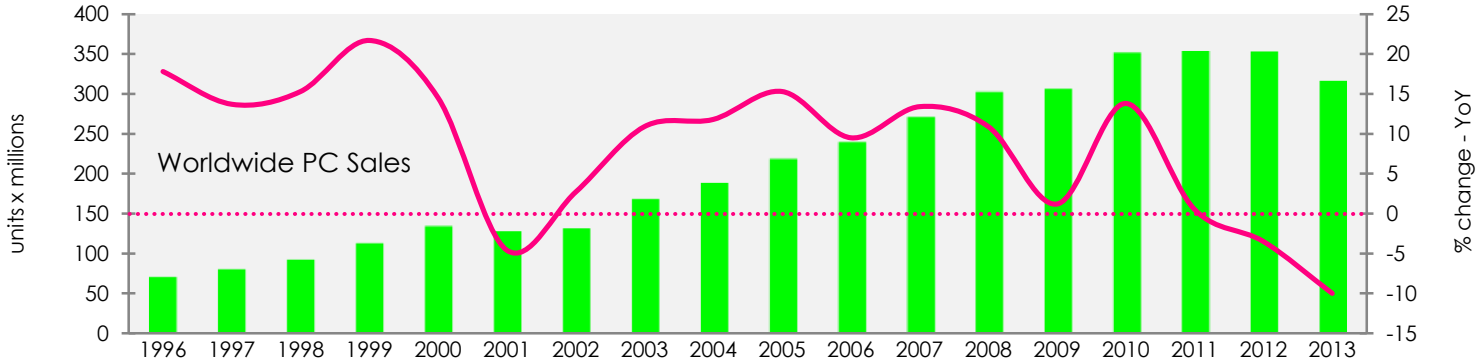
Computer Market Disruption

- Welcome to the "Post PC Era"
  - 7 consecutive quarters of decline, 2012-2013 -10% Year-on-Year
  - Smartphones >50% share of mobiles in 2013, billion unit market
  - Low cost "hybrid" tablet/PCs and Chrome Book PCs emerging
  - Software as a Service and Cloud Computing rapidly replacing the packaged software application paradigm
  - "Internets of Things" = explosion of modules everywhere



	1996	1997	1998	1999	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013
Unit Sales	70.9	80.6	92.9	113.5	134.7	128.1	132.4	168.9	189	218.5	239.4	271.2	302.2	305.9	351	352.8	352.7	316
Growth %	17.8	13.7	15.3	21.7	14.5	-4.6	2.7	10.9	11.8	15.3	9.5	13.4	10.9	1.2	13.8	0.5	-3.5	-10

Gartner 1995 - 2013

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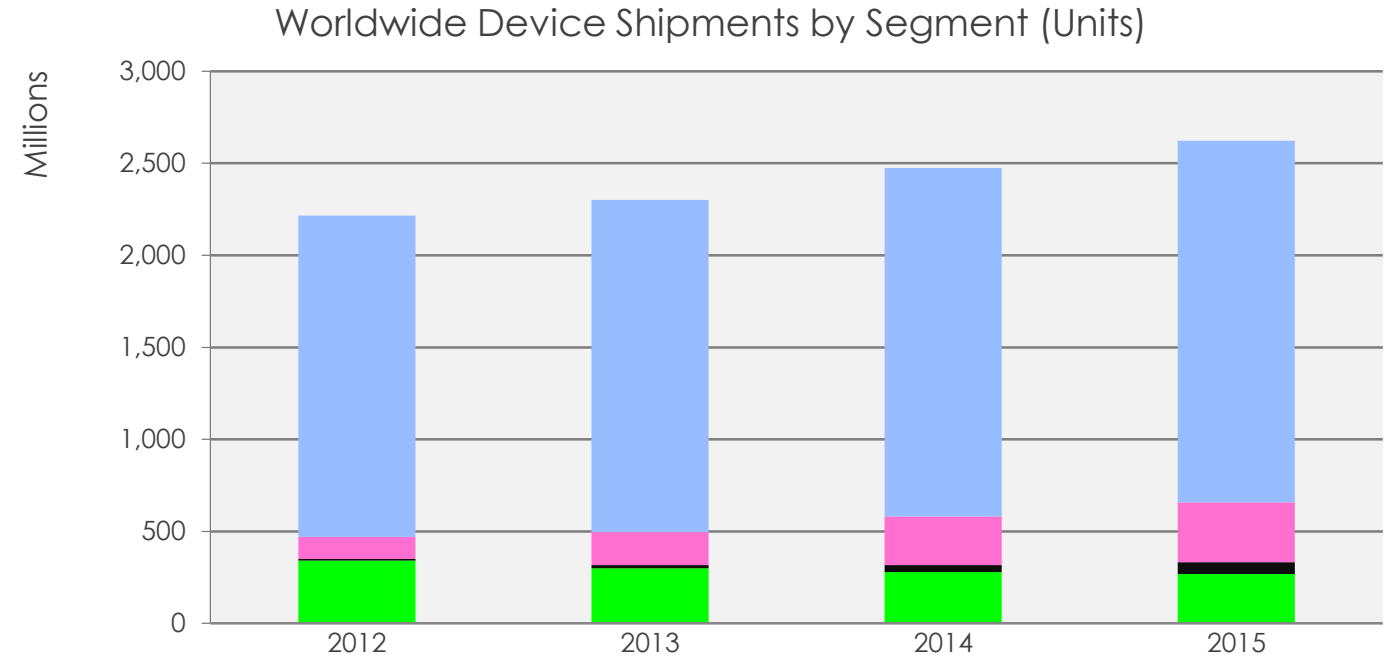
User Device Market Trends



	2012	2013	2014	2015
Mobile Phone	1,746,177,000	1,804,334,000	1,893,425,000	1,964,788,000
Tablet	119,529,000	179,531,000	263,450,000	324,565,000
Ultramobile	9,344,000	17,195,000	39,636,000	63,835,000
PC	341,273,000	299,342,000	277,939,000	268,491,000

Gartner 2014 Jan 07 - http://www.gartner.com/newsroom/id/2645115

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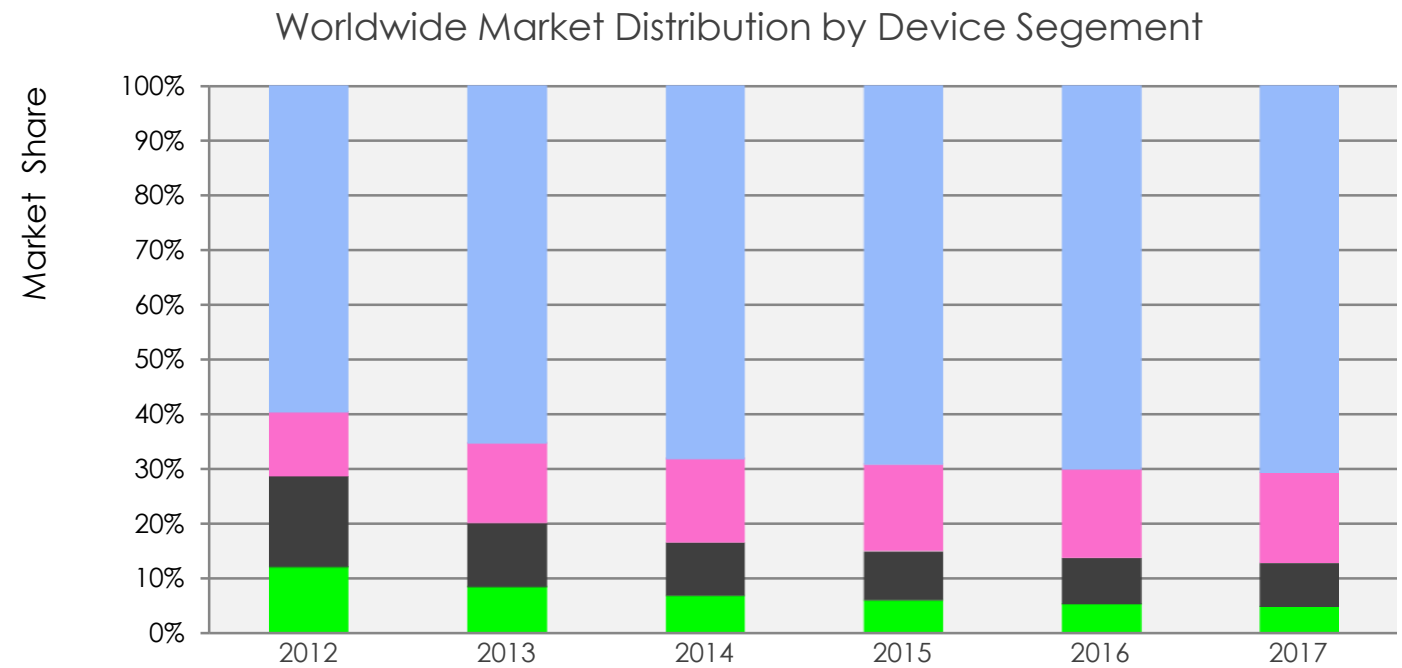
User Device Market Trends



	2012	2013	2014	2015	2016	2017
Smartphone	59.46	65.17	67.97	69.04	69.82	70.47
Tablet	11.81	14.61	15.34	15.86	16.26	16.54
Notebook PC	16.52	11.61	9.69	8.93	8.41	7.99
Desktop PC	12.21	8.61	7.00	6.17	5.51	5.00

Source : IDC 2013 Sept 11 - http://www.idc.com/getdoc.jsp?containerId=prUS24314413

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Modular Computing Technology

Intel ® NUC Next Unit of Computing

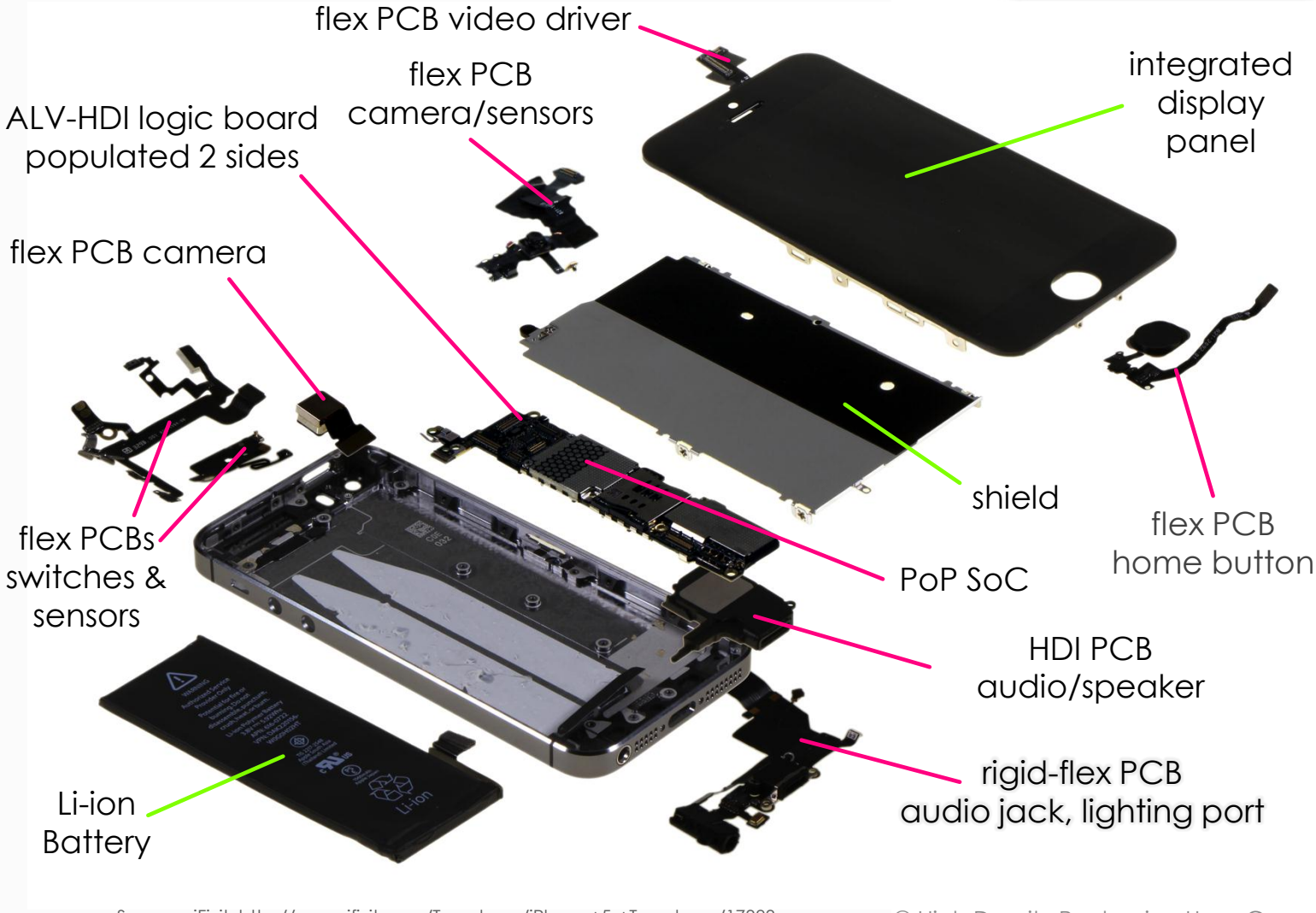
Conventional MLP & HDI
Trending to stacked via BGA

Open Compute Project
"vanity-free" processor sled

DIY - add your own DDR3, wireless, SSD or HDD

Intel ® NUC Next Unit of Computing
Ars Technica – 2014 Jan 06

Hand Held Technology



Source : iFixit http://www.ifixit.com/Teardown/iPhone+5s+Teardown/17383

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CSP Ball Pitch Design Rules

Variable	0.80mm	0.60mm	0.50mm	0.40mm	0.30mm
CSP Ball Diameter	460um	275um	275um	240um	210um
NSMD Copper Pad Diameter	450±25	265±20um	265±20um	225±20um	160±15um
NSMD Soldermask Diameter	550±25	375±25um	375±25um	325±20um	220±15um
Overlay Tolerance (max)	±50	±50	±50	±40	**±20**
Peripheral Routing Escape Lines/Channel x Width	1 x 100um 2 x 70um	1 x 100um 2 x 60um	1 x 75um **2 x 40um**	1 x 50um **2 x 35um**	1 x 40um
Via Interconnect Escape	Staggered or Via in Pad	Staggered or Via in Pad	Staggered or Via in Pad	Staggered or Via in Pad	Via in Pad
SMD Copper Pad Diameter	550±25	375±25um	375±25um	325±20	220±15um
SMD Soldermask Diameter	450±25	265±20um	265±20um	225±20	160±15um
Overlay Tolerance (max)	±50	±50	±50	±40	**±20**
Peripheral Routing Escape Lines/Channel x Width	1 x 80um **2 x 50um**	1 x 70um **2 x 40um**	**1 x 40um**	**1 x 25um**	**1 x 25um**
Via Interconnect Escape	Staggered or Via in Pad	Staggered or Via in Pad	Staggered or Via in Pad	Via in Pad	Via in Pad

Standard HDI (e.g., 1+, 2+)

Advanced HDI (3+ … ALV)

Advanced HDI Roadmap

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BGA Design Rules (microns)

BGA Pitch	Signal Routing	Inner Line	Inner Space	Laser Via	Inner Pad	Outer Pad	SM Opening	Remarks
0.40mm	1 Track	0.7	-	100	200	225	300	JISSO Roadmap
0.40mm	1 Track	60	65	75	200	200	275	Current Practice
0.40mm	2 Track	40	45	75	180	180	255	Next Gen High I/O SoC, requires mSAP
0.30mm	1 Track	50	-	75	150	240	175	JISSO Roadmap
0.30mm	1 Track	50	50	75	200	240	175	Current Practice
0.30mm	2 Track	30	30	75	150	240	175	Forecast, requires mSAP
0.25mm	1 Track	50	50	50	100	-	-	JISSO Roadmap, requires mSAP
0.15mm	1 Track	25	25	30	75	-	-	JISSO Roadmap, requires coreless & SAP

@ limit or beyond subtractive process

Dielectric Thickness (microns)

Min BGA	Signal Routing	Core Layer	Build-up Layer	Total Layers	Remarks
0.40mm	1 Track	60	60	10	Current Practice STD HDI
0.30mm	1 Track	50	45	10 ~ 12	Current Practice ADV HDI
0.30mm	2 Track	40	40	10 ~ 12	Next Generation ADV HDI
0.25mm	1 Track	40	30 ~ 35	10 ~ 12	Forecast 2015-2016

@ limit of existing FR4

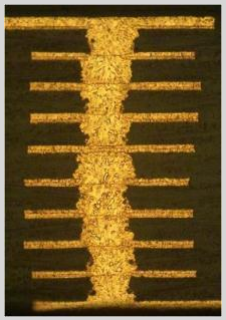
beyond limit of existing FR4

HDI / ALV Design Trends

No Change ???

- Handheld/wearable electronic packaging:
  - Design envelope dominated by batteries & displays
  - Miniaturized & modularized PCBA design with high flex content
  - Extensive use of SoC design, with SiP, PoP & WCSP packaging
  - Low profile CSP, WCSP & microQFN devices, 0.40~0.30mm pitch
  - Ultra-thin 8-14 Layer HDI PCB design, current and near term:
    - Via in Pad/stacked via ICT with decreasing pad diameter
    - Conductor line/space design rules approaching 40/60
    - 2 track routing in 0.40umm pitch devices up to 36x36 BGA
    - 25~40um dielectrics
    - 250~800um thickness
    - Flex & coreless HDI

How does the performance & reliability stack-up?



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Problem Statement

- Methods & test vehicles lag design by a decade
  - Do not capture interconnect density or thinness
  - Miss potential failure mechanisms (e.g., ion migration)
  - Low density patterns introduce artifacts not seen in production (e.g., laminate voids, localized distortion)
  - Standard test parameters may exceed limits of design
  - Standard test vehicles abandoned by OEMs in favor of non-standard "end product" test vehicles
  - Widens gaps between up-stream development & product design; back-end product testing before launch a is high risk strategy
  - Major OEMs work in a black box expecting component, PCB & material supply-chain actors to provide solutions from a vacuum

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Project Proposal

- Design, test & standardize an open-source HDI test vehicle for qualification of materials, components, PCBs & PCBA
  - Scaled to smartphone form factors
  - Modularized, based on 50mm x 50mm increments for various mixes of bare board & assembly TVs
  - 0.40, 0.35, 0.30 & 0.25mm pitch BGA devices
  - 01005 (and smaller?) chip passives
  - 40/60um nominal line/space design rules
  - All Layer Via interconnect with stacked vias, Via in Pad
  - 12 layer build-up with alternating plane/signal pattern density
- Deliverables: TV Design, test build & test report
- Duration : 12-16 months (depending on duration of tests)

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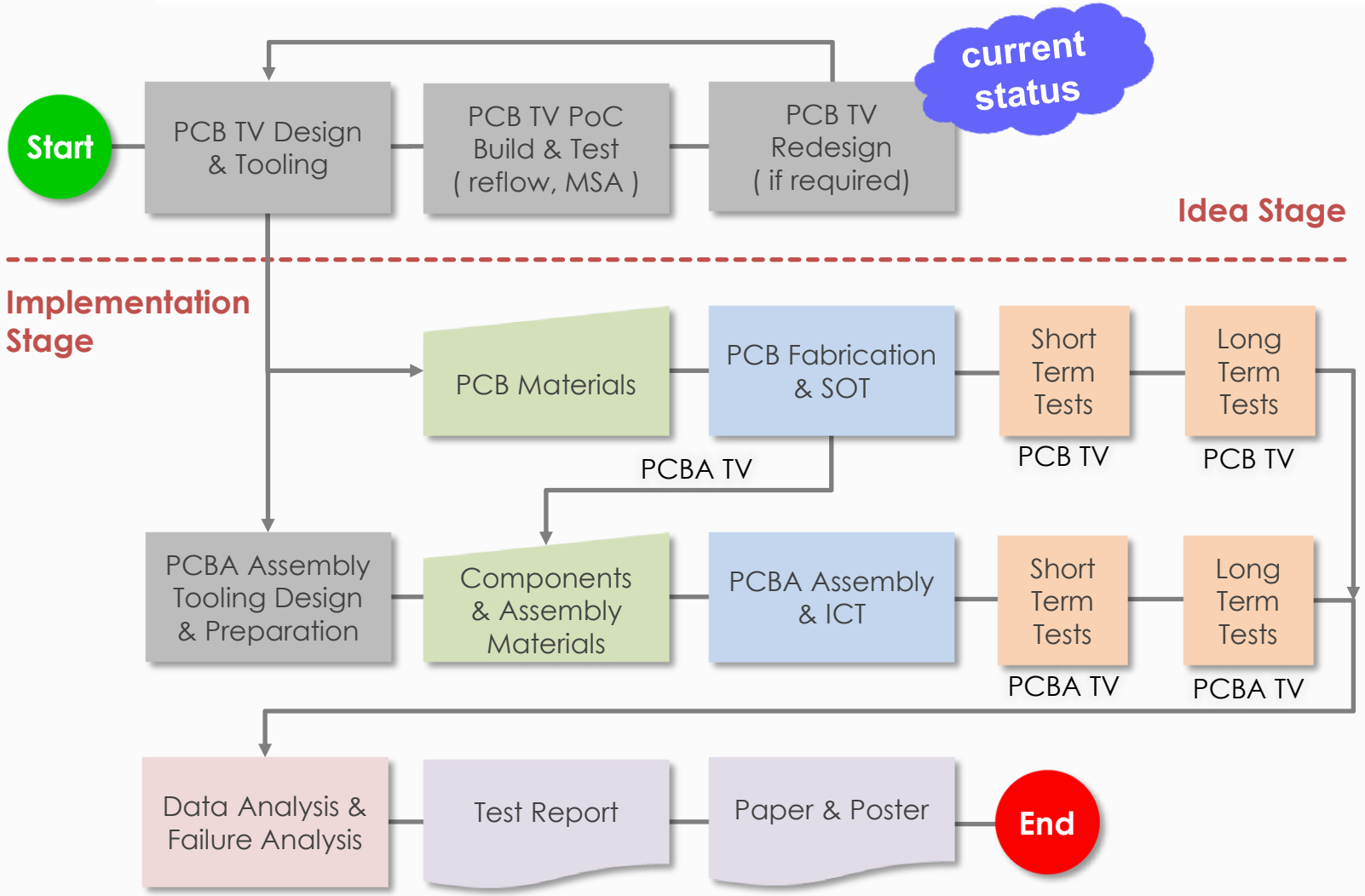
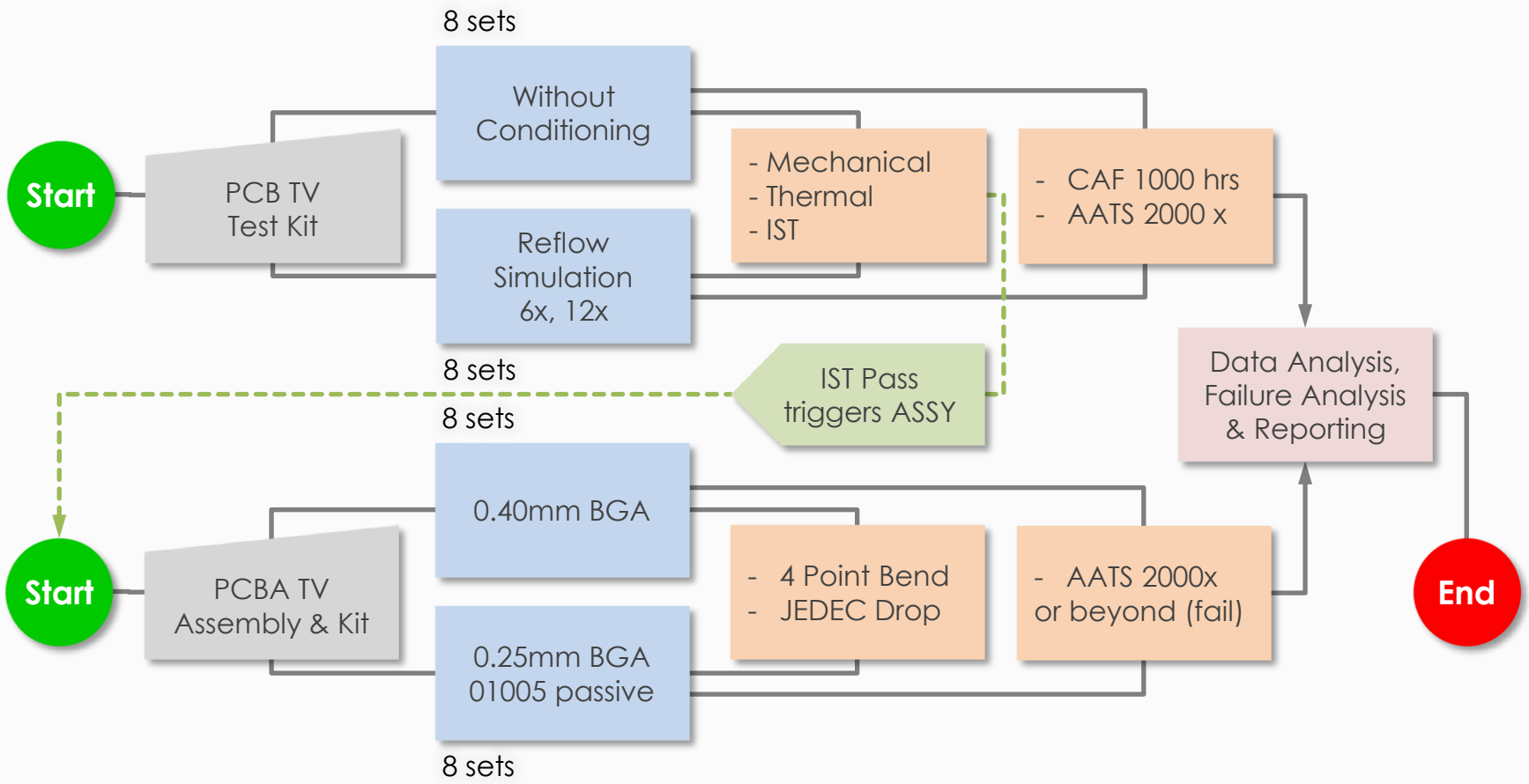
General Project Work Flow



Test Work Flow



Project Task List

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Tasks		Item	Company	Responsible	Status	Start	End
Idea Stage Project	Org.	Project Idea Proposal	TTM, TI	Katzko, Nguyen	Complete	2012.12.05	2012.12.05
		Organization, Recruitment & Kick-off	HDPUG, TTM	Smith, Katzko	Complete	2013.02.26	2013.06.19
	Design	Preliminary TV Design Proposal (generic)	TTM	Katzko, Lee et al	Complete	2013.07.10	2013.07.24
		PCB Coupon Set Specification & Floor Plan	Panasonic, TTM	Senese, Katzko et al	Complete, subject to change in design	2013.07.24	2013.09.04
		PCB Coupon Set CAD Design	TTM	Lee, Xiao	Working - started September 23	2013.09.23	2013.10.11
		PCB Coupon Set Design Review	Project Team	Team	Pending CAD completion	2013.10.16	2013.10.30
		PCB Proof of Concept Build	TTM	Lee, Han	Complete	2013.11.04	2013.11.22
		PCB Proof of Concept Validation-Debugging	TTM	Han, Huang, Xiao	Redesign in progress	2013.12.09	EST 2014.03.14
		PCBA Coupon Set Specification & Floor Plan	Engent, TTM	Xie, Katzko, Lee	Complete	2013.07.24	2013.12.04
		PCBA Coupon Set CAD Design	Engent, TTM	Xie, Katzko, Huang	Working	EST 2013.12.09	EST 2014.03.13
		PCBA Coupon Set Design Review	Project Team	Team	Pending	EST 2014.03.19	EST 2014.03.26
		PCBA Proof of Concept Build -	TTM	Lee, Han	Pending	EST 2014.03.31	EST 2014.04.14
		PCBA Proof of Concept Validation Tests		Han, Huang, Xiao	Pending	EST 2014.04.14	EST 2014.04.21
	BOM	Test Proposal & BOM Parts Estimation	Engent, TTM	Katzko, Team	Preliminary proposal under preparation	EST 2014.03.24	EST 2014.03.31
		PCB Materials Specification & Estimation	TTM, Panasonic	Katzko, Senese	Preliminary proposal under preparation	EST 2014.03.24	EST 2014.03.31
Implementation Stage Project		PCB Materials Sourcing	Panasonic	Senese	Donated materials	TBD in March	TBD in March
		BGA/WCSP Daisy-Chain Sourcing	Donate/Purchase	Katzko, Smith	Pending - needs proposal & budget	TBD in March	TBD in March
		Passive Device Sourcing	Donate/Purchase	Katzko, Smith	Pending - needs proposal & budget	TBD in March	TBD in March
	Build	PCB Test Vehicle Fabrication	TTM	Han	Pending - 2 weeks lead time	TBD in March	TBD in March
		PCBA Assembly & SOT	Engent	Xie	Pending - 4 weeks lead time	TBD in March	TBD in March
	Test	Performance & Reliability Test Tasking	HDPUG, TTM	Katzko, Smith	Pending - 2 weeks planning time	TBD in March	TBD in March
		PCB Testing & Analysis	TBD	Katzko, Smith	Pending - 10 weeks (AATS may extend)	TBD in March	TBD in March
		PCBA Testing & Analysis	TBD	Katzko, Smith	Pending - 10 weeks (AATS may extend)	TBD in March	TBD in March
	Pub.	Report Preparation	Project Team	Katzko, Team	Pending - 4 weeks lead time	TBD in March	TBD in March
		Paper & Poster Preparation	Project Team	Katzko, Team	Pending - 2 weeks lead time	TBD in March	TBD in March
						22 - 26 weeks implementation	

Define March 2014

Active Participants

Engent	Fei Xie	
Kyzen	Mike Bixenmann	
Panasonic	Tony Senese	
TTM	Tommy Huang	
	Angela Lee	
	Summer Xiao	
	C.B. Katzko	Project Leader
HDPUG	Ruben Bergman	
	Robert Smith	Project Facilitator

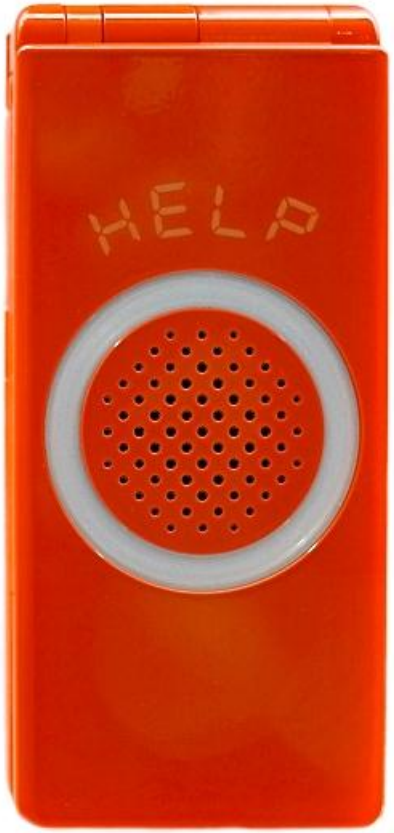
Supporters & Friends

Alcatel-Lucent	Joseph Smetana
Boeing	Kenneth C. Noddings
Curtiss-Wright	Ivan Straznicky
Engent	Dan Baldwin
	Paul Houston
Flextronics	Jennifer Nguyen
HDPUG	Jack Fisher
	Lawrence Schultz
	Marshall Andrews
Hitachi Chemical	Ken Hikida
	Takahiro Tanabe
Isola	Fred Hickman

ITEQ	Robert Hung
Kyzen	Mike Bixenmann
Nihon Superior	Keith Howell
Panasonic	Abe Tomoyuki
Park Electro	Silvio Bertling
Poltronic	Paul Collander
Sekisui	Hiroya Ishida
Shengyi Sytech	Kevin Zhang
TTM Technologies	Zaron Huang
	Marika Immonen
	Tarja Rapala
Texas Instruments	Luu Nguyen
TUC	Alan Cochrane

Want Ad

- Member Support
  - Device ODMs (design input, review, dotation)
  - PCB designers (design input/review)
  - Captive or Independent test labs (work)
- Material Resources
  - Daisy-chain devices (donated or purchased)
  - Passive devices (donated or purchased)
  - Assembly materials suppliers (solder, Underfill)
  - Test services
- Working Timeline/Commitment
  - Design 3-4 months (covered)
  - PoC Lot Fabrication & Test 1 month (done)
  - PCB Fab, Assembly & Test 6-9 months



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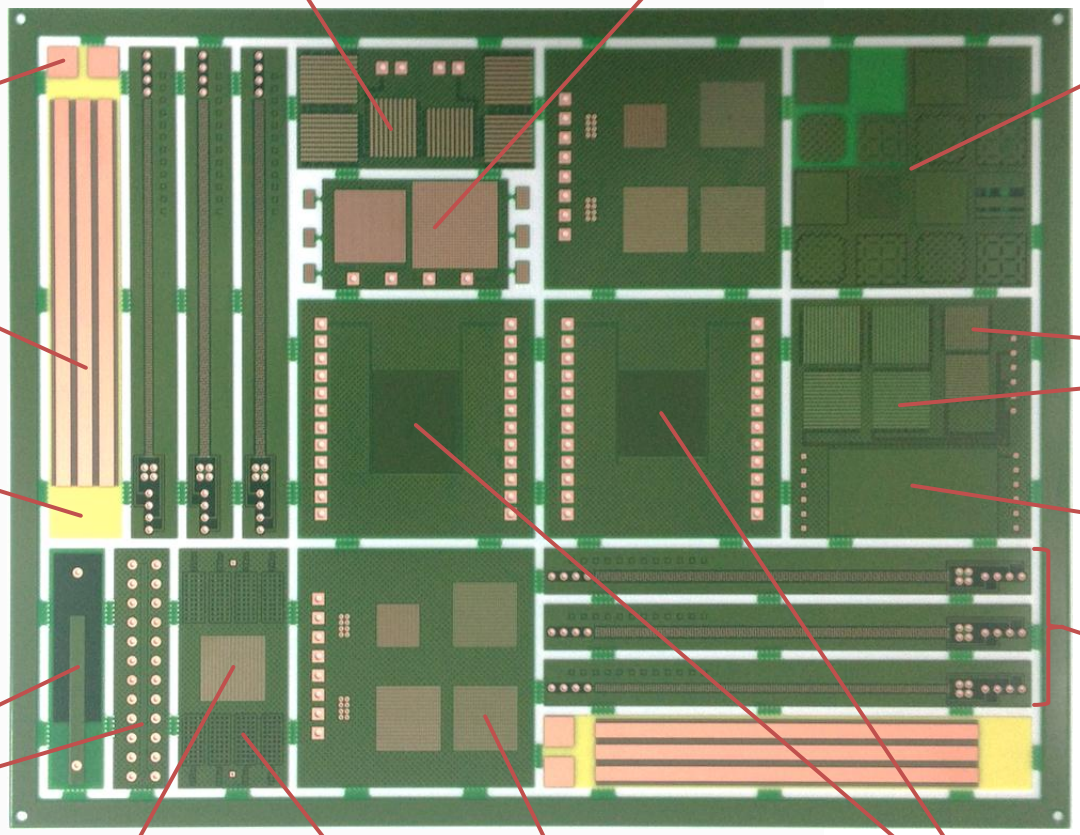
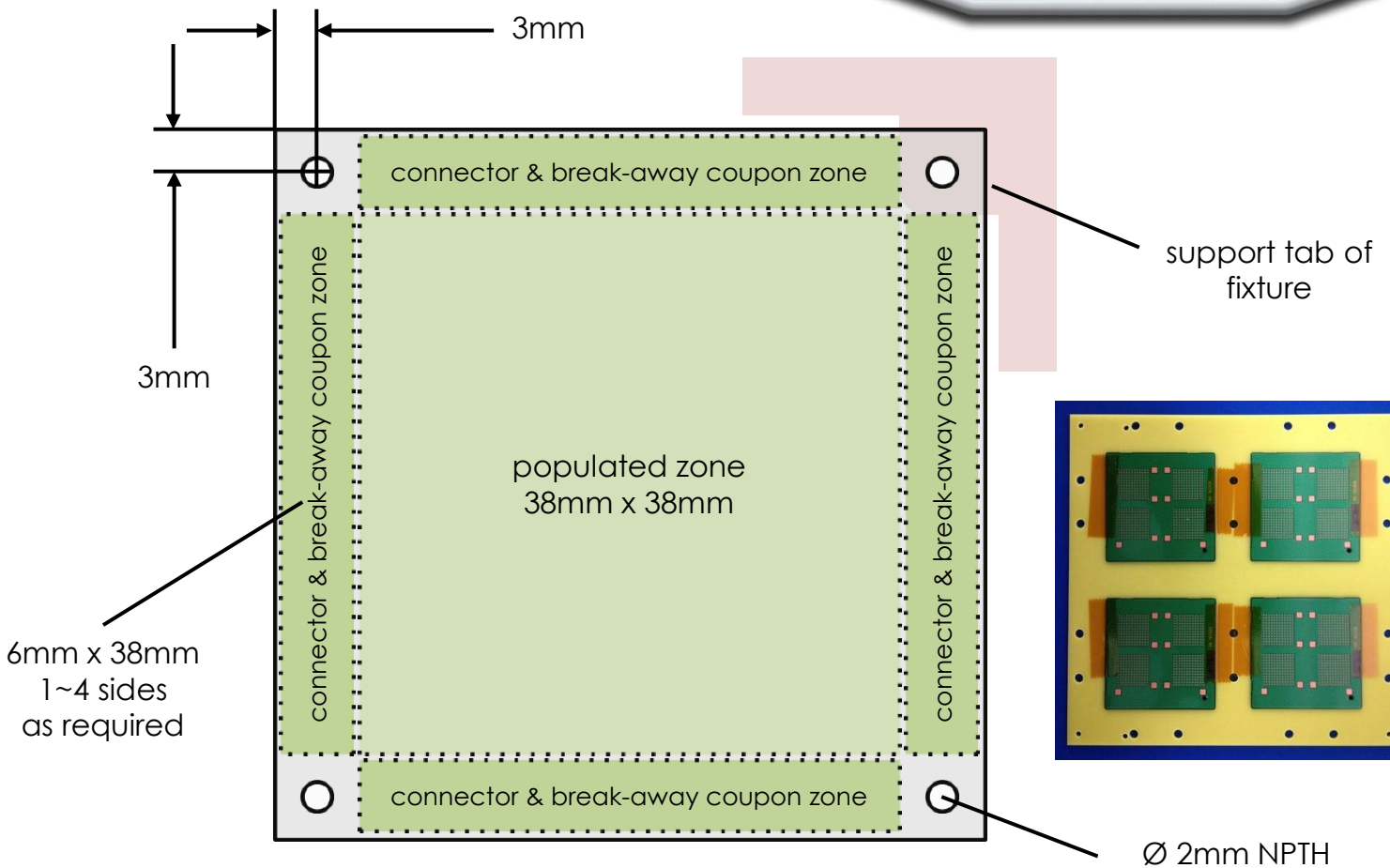
Test Vehicle Design Progress

PCB TV Proof of Concept Build

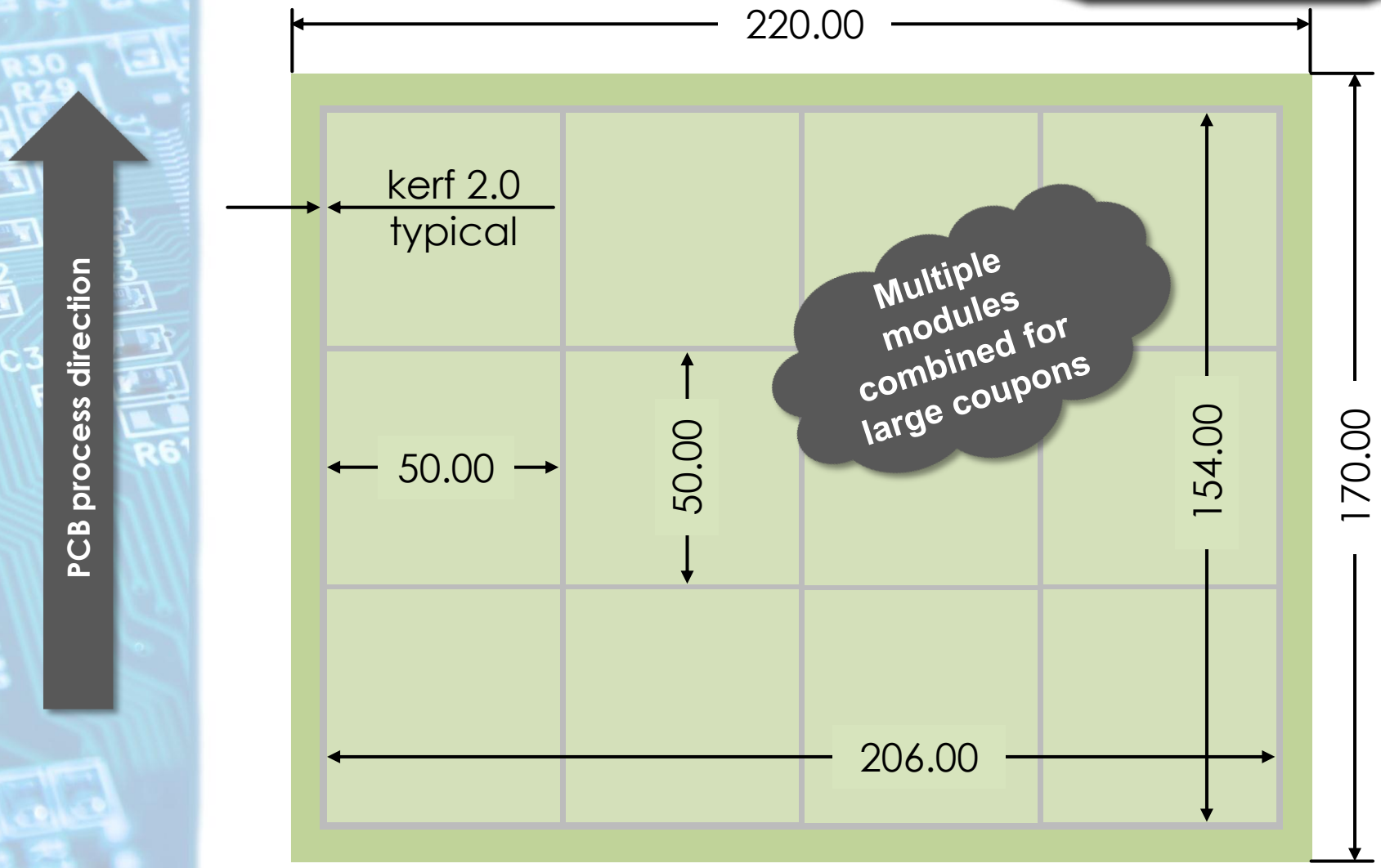


50 x 50mm Module

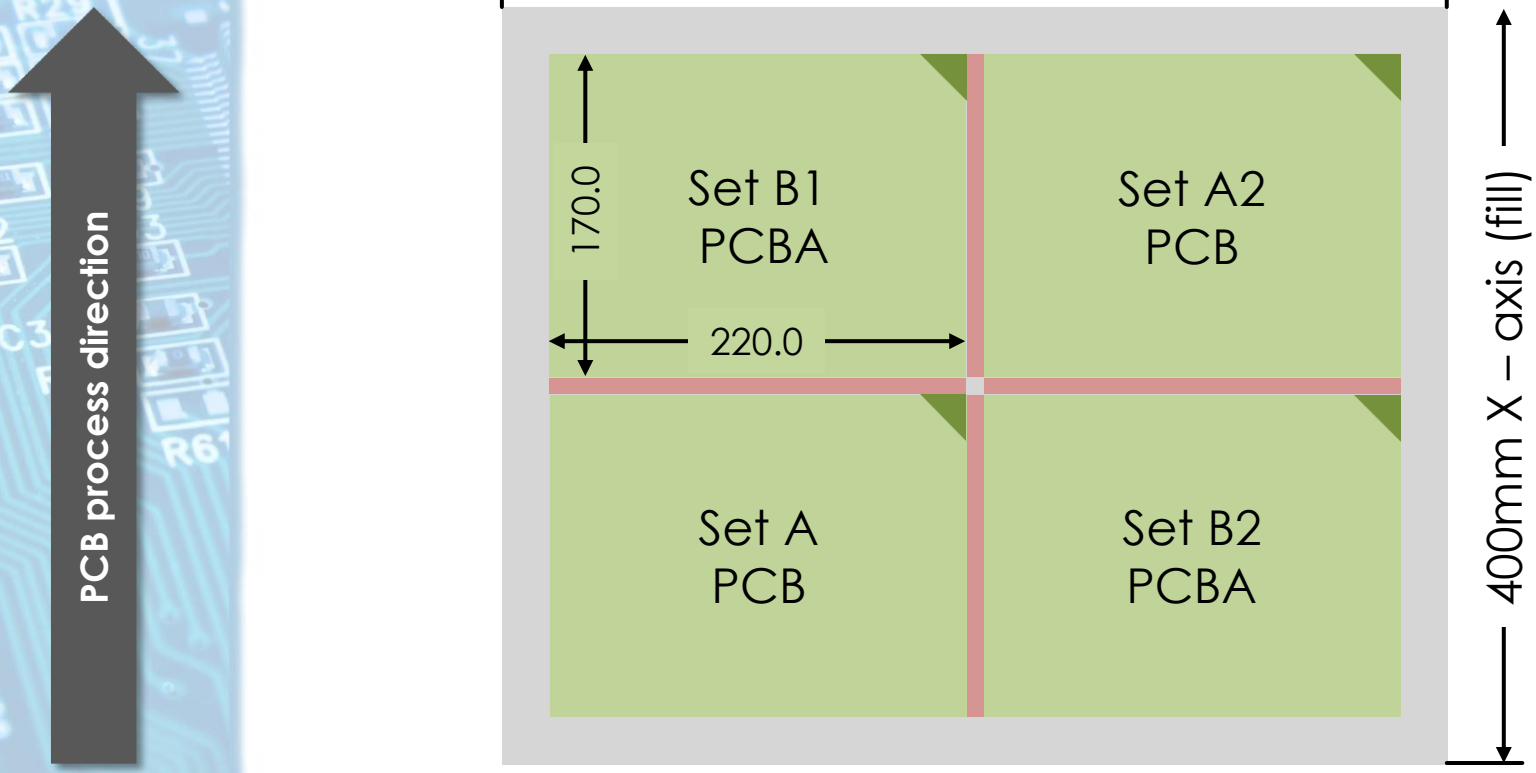


Connectors : 2.54mm pitch
Wire : 26 AWG or 28 AWG
Pins : Typically 0.50mm square
PTH : Ø1.05mm (1.2mm drill)

Set Design


220.00
kerf 2.0
typical
Multiple modules combined for large coupons
50.00
50.00
154.00
170.00
206.00
PCB process direction

Panel Layout



- 2 set designs, “PCB test” & “PCBA” test, 2+2 sets per panel
- Sets step diagonally opposite, “inside” & “outside”
- “PCBA Test” sets can be divided into sub-sets for assembly

PCB Floor Plan

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Soldermask | No Soldermask

Y-axis (warp)

X – axis (fill)

PCB process direction

Hipot coupon

Cold Ball Pull/Shear + Monotonic Bend (no SM) + Cold Ball Pull/Shear

4 P connector | 4 P connector

micro section: AATS 0.40mm 30 x 30 Pad Size A | AATS 0.40mm 30 x 30 Pad Size B: micro section

micro section: AATS 0.30mm 30 x 30 Pad Size A | AATS 0.25mm 30 x 30 Pad Size A: micro section

4 P connector | 4 P connector

Peel Strength Y-axis (w 15mm x L 101.5mm, 3 conductors W 3mm x 80mm)

micro section: IST Y-axis Stacked Via 0.40mm, 0.25mm pitch/Through Via 0.5mm pitch: micro section

Peel Strength X-axis (w 15mm x L 101.5mm, 3 conductors W 3mm x 80mm)

IST X-axis Stacked Via 0.40mm, 0.25mm pitch/Through Via 0.5mm pitch

12 P connector

Line/Line CAF 75um/75um

12 P connector

12 P connector

Line/Line CAF 75um/50um

12 P connector

6 P connector | 4 P connector

6 P connector: Layer/Layer CAF | Via/Via CAF 0.40mm X - Y: micro section

micro section: Via/Via CAF 0.30mm X - Y | Via/Via CAF 0.25mm X - Y: micro section

4 P connector | 4 P connector

4 P connector | 4 P connector

micro section: AATS PTH 0.60mm 30 x 30 Φ 0.25mm | AATS PTH 0.50mm 30 x 30 Φ 0.25mm: micro section

micro section: PTH/PTH CAF 0.60mm X - Y | PTH/PTH CAF 0.50mm X - Y: micro section

4 P connector | 4 P connector

4 P connector | 4 P connector

micro section: AATS 0.40mm 30 x 30 Pad Size A | AATS 0.40mm 30 x 30 Pad Size B: micro section

micro section: AATS 0.30mm 30 x 30 Pad Size A | AATS 0.25mm 30 x 30 Pad Size A: micro section

4 P connector | 4 P connector

Multi Pattern Delam

Multipurpose Checkerboard with/without copper for DSC, TMA, TGA

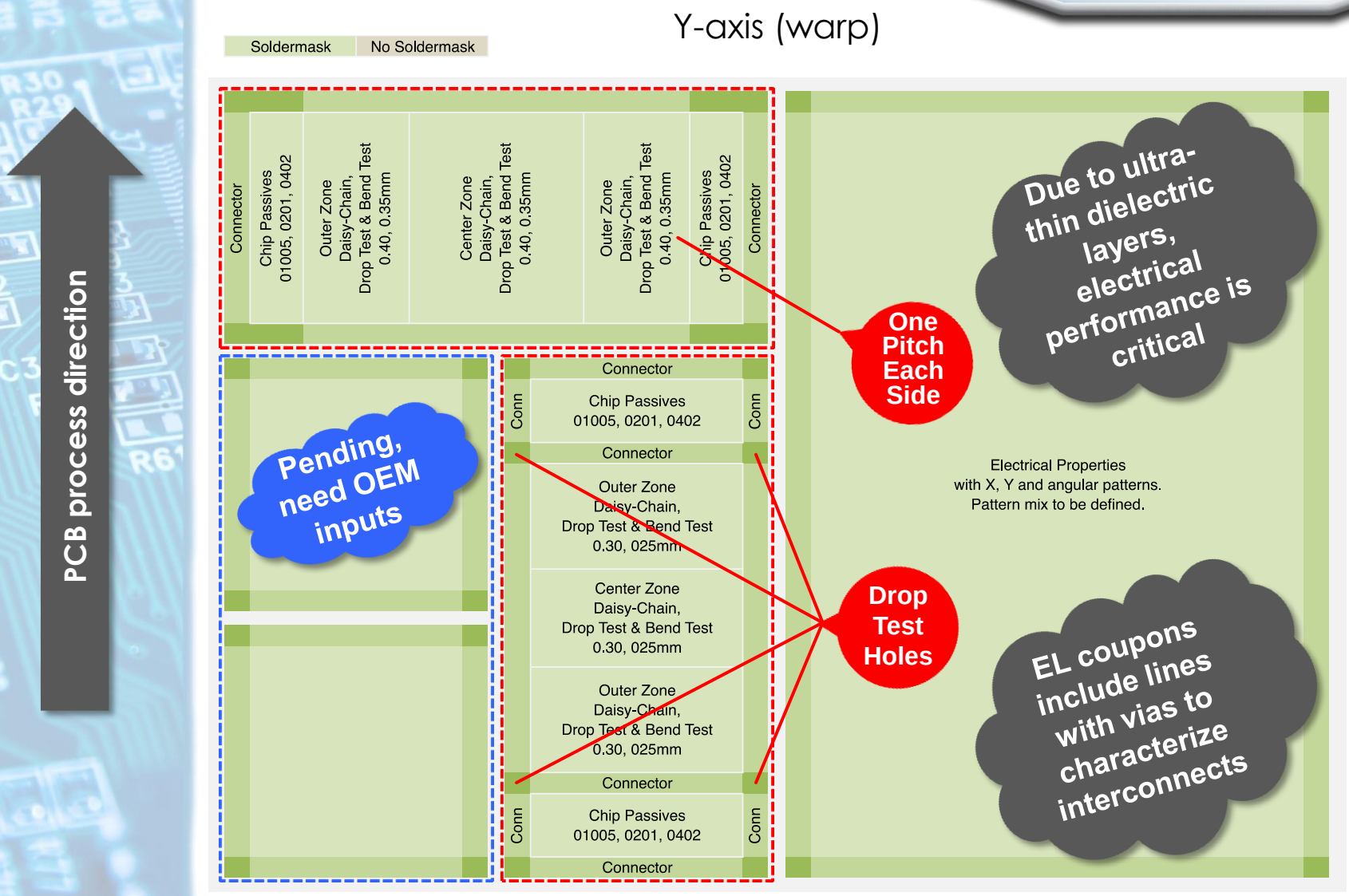
DMA

DMA

DMA

Under Redesign

PCBA Floor Plan



12 Layer Build-up

- Typical logic board design is 10-14 layers
- 12 layers is best match to electrical & IST coupons
- 1037 construction for proof of concept builds

Confirmed for Design

	Layer	Material Type	Target Thickness um	Description	Cu Density
Build-up Layers	1	9um Cu Foil + Cu Plating	25	SMD Assembly	-
		1x1067, 1037 or 1027	0.4	Prepreg Dielectric	
	2	9um Cu Foil + Cu Plating	18	Plane	75%
		1x1067, 1037 or 1027	40	Prepreg Dielectric	
	3	9um Cu Foil + Cu Plating	18	Signal	50%
		1x1067, 1037 or 1027	40	Prepreg Dielectric	
	4	9um Cu Foil + Cu Plating	18	Plane	75%
		1x1067, 1037 or 1027	40	Prepreg Dielectric	
	5	9um Cu Foil + Cu Plating	18	Signal	50%
		1x1067, 1037 or 1027	40	Prepreg Dielectric	
Core	6	9um Cu Foil + Cu Plating	18	Plane	75%
		0.60mm 1x1067 or 1080	60	Core Dielectric	
Build-up Layers	7	9um Cu Foil + Cu Plating	18	Plane	75%
		1x1067, 1037 or 1027	40	Prepreg Dielectric	
	8	9um Cu Foil + Cu Plating	18	Signal	50%
		1x1067, 1037 or 1027	40	Prepreg Dielectric	
	9	9um Cu Foil + Cu Plating	18	Plane	75%
		1x1067, 1037 or 1027	40	Prepreg Dielectric	
	10	9um Cu Foil + Cu Plating	18	Signal	50%
		1x1067, 1037 or 1027	40	Prepreg Dielectric	
	11	9um Cu Foil + Cu Plating	18	Plane	75%
		1x1067, 1037 or 1027	40	Prepreg Dielectric	
	12	9um Cu Foil + Cu Plating	25	SMD Assembly	-
			650.4		
			Total Thickness		

high density & thickness yield

low density & thickness yield

NB - Prepreg resin content % requires adjustment based on copper pattern density

Thank You

Q&A

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