HDP User Group International, Inc.

TSV Project

Status

Dave Love

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Trying a New Approach

- Very little progress in 2013
- A 2.5D TSV project requires test chips and interposers
- These have been very difficult to obtain through our usual way of doing things.
- Suppliers don't want to collaborate with competitors after heavy financial investment
- Suppliers don't want their dirty laundry exposed
- Suppliers don't want to share their IP
- The new approach: Single Supplier Projects
  - Offer a safe environment for IP
  - Single-source each type of component
  - Offer access to our strengths in board assembly and reliability testing

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Current Status

- Trying the new approach since November
- Simultaneously, Larry and Marshall have been talking to Freescale
- Freescale offered to provide test chips (2 types) to the project - but we need to source the interposer
- Dave and Larry talking to interposer suppliers now
- One interposer supplier (RTI) has a new project with a 2.5D interposer and FPGA and Memory chips - in layout now
- RTI interested in collaboration if HDP can provide the board-level reliability work
- So, we may have two parallel projects - we will follow up on both

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Freescale Test Chips Description

- 2 test die designs, both to tape out this quarter
- Interposer floor plan will have 4 of die #1 and 1 of die #2
- Thermal characterization: both die have heaters and die #2 also has hot spot capability
- Both die are 28nm and therefore use ultra-low-K dielectric
- There are daisy chains incorporated to test all levels of interconnect together and separately
- The interposer will be 18 x 28 mm, intended for 65nm
- 40,000 TSVs on the interposer
- Pitches range from 40um (microbump) to 180um (power/ground)

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Motivation to Collaborate

- Our membership includes numerous system-level package users.
- IC suppliers, interposer suppliers, and wafer fabs don't spend many engineering resources on system-level issues such as SMT assembly process and board-level reliability.
- But this information is vital to generate product acceptance in the marketplace.
- Partnership of package users and package suppliers can find fertile common ground for collaboration.
- IF: we can address their concerns

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Suppliers' Concerns and Needs

- Protect their IP and sensitive information
- Remember that this is NEW technology and there will be hiccups
- Don't publish suppliers' dirty laundry (e.g. ugly cross sections, early failures)
- Control sharing with competitors
- Help the suppliers' customers with SMT process characterization and guidelines
- Help suppliers to understand package-, board-, and system-level requirements
- Help suppliers to understand the package and board-level effects on their product reliability

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What does HDPUG have to offer?

- 2.5D assembly services
- PCB design and procurement
- SMT Process Characterization report
- SMT Process Guidelines document
- ATC testing and failure detection
- Monotonic bend testing and failure detection
- Drop-shock and vibration testing
- Sensitive TSV-level fault detection (NIST)
- Thermal analysis and models at system level
- Failure analysis (cross sections, SEM, etc.)
- Mechanical modeling
- Final report

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What does HDPUG need?

- IC test vehicles
- 2.5D Interposer
- Drawings and net-list of test vehicle.
- Optimum test vehicle would have:
  - Power cycling capability
  - 4-point access for NIST test, if required
  - Design for F/A
- Material properties and geometries for modelling

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Outputs of the Project

- 2.5D Package Assembly Characterization
- Package-level Reliability Report
- Detailed SMT Assembly Characterization Report
- SMT Assembly of 2.5D Packages Guideline Document
- Board-level Reliability Report
- Board-level Mechanical Stress Models of 2.5D Package
- Thermal Resistance Report, empirical + model

Note: any of these can be published as Journal or Conference papers, if all contributors agree

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Suppliers of Interest - Status

	Category	STATUS 2/13
Amkor	OSAT Package Assembler	
ASE	OSAT Package Assembler	
Engent	OSAT Package Assembler	HDP Member
Stars Microelectronics	OSAT Package Assembler	Invitation to project sent
Xilinx	Early Adopter	Invitation to project sent
Altera	Early Adopter	Invitation to project sent
Freescale	Early Adopter	Coming to Feb HDP meeting
eSilicon	Early Adopter	
AMD	Early Adopter	
SK Hynix	Early Adopter	
Teradyne	Early Adopter	
Renesas	Early Adopter	
IPDIA	Interposer	Discussed project 1/30
Allvia	Interposer	Invitation to project sent
RTI	Interposer	Discussed project 2/11
Silex	Interposer	Coming to Feb HDP meeting
Tezzaron	Interposer/3D Die	Invitation to project sent
Invensas	Interposer/3D Die	Invitation to project sent
TSMC	Interposer/3D Die	No response to contact
UMC	Interposer/3D Die	No response to contact
Global Foundries	Interposer/3D Die	Invitation to project sent

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Task List - Freescale 2.5D Project

- Freescale provide test die (2 types) and netlist
- HDPUG to source the interposer, including design and fab
- HDPUG to ensure NIST test structures are present
- IC assembly to the interposer including encapsulation and termination metals (Engent)
- Define all stress tests and measurements (NIST, Engent)
- Package-level stress testing (ATC, THB, HTS...?) including fault detection
- Perform thermal resistance testing (Freescale)
- PC board layout and procurement
- SMTA assembly of 2.5D package on PCB
- SMTA process characterization report
- Board-level stress testing (ATC, Monotonic Bend, Shock/Vibe) including fault detection
- Weibull analysis
- Failure Analysis
- Thermal and/or Mechanical modeling

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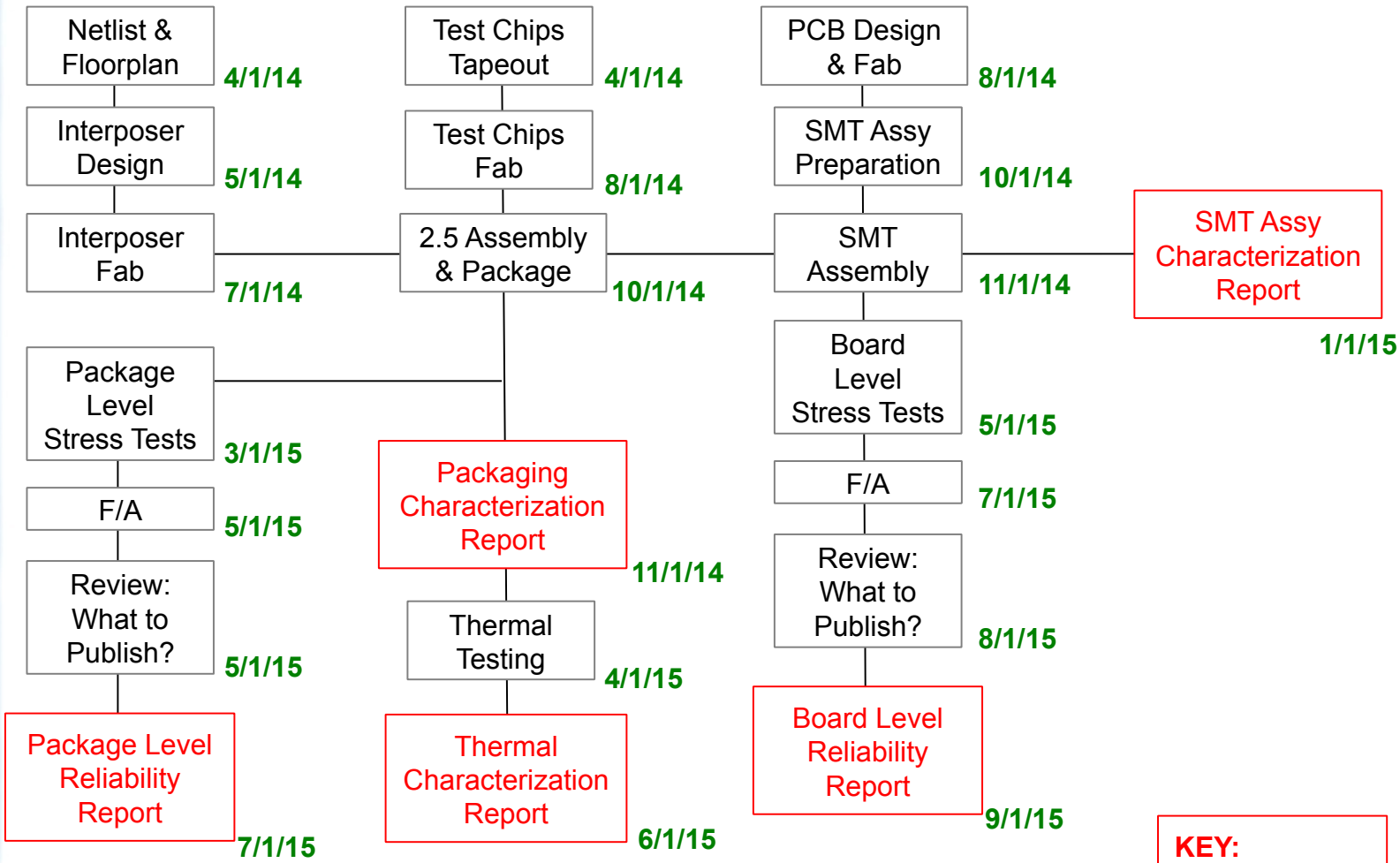
Draft Project Flow and Schedule



KEY:
Red boxes are OUTPUTS

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