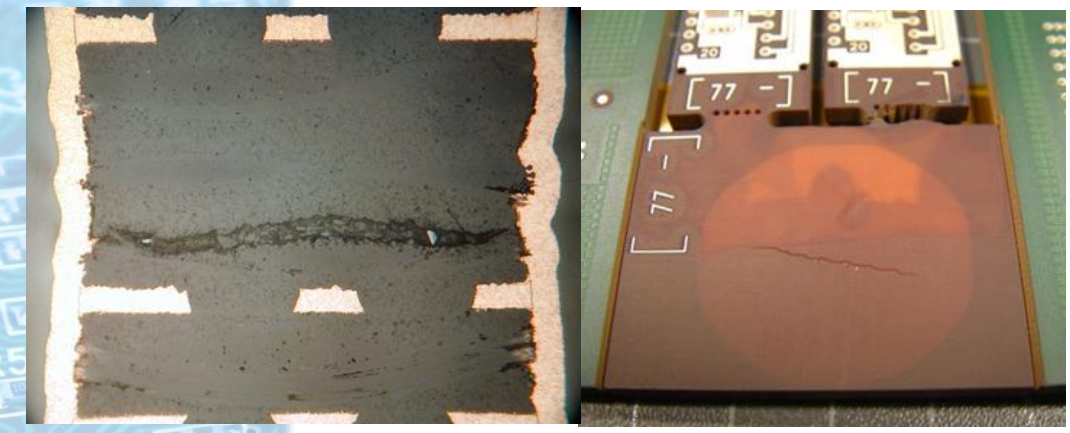
Pb-free PWB Materials Reliability Phase 4

Project Leader : John Wilson, IBM
Project Facilitator : Brian Smith, HDP User Group

26th February 2014

The Problem : Potential Issues Caused By Pb –Free SMT Reflow



Internal & Surface Delamination

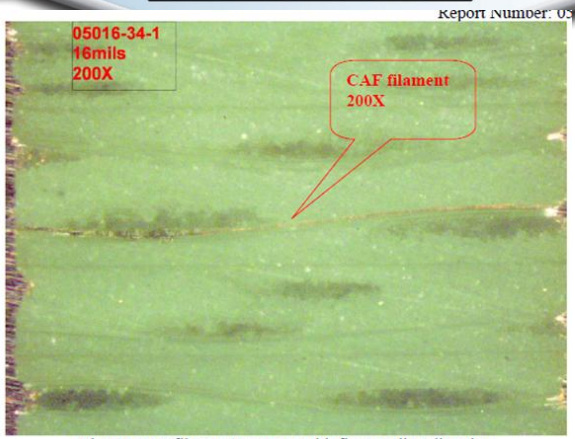
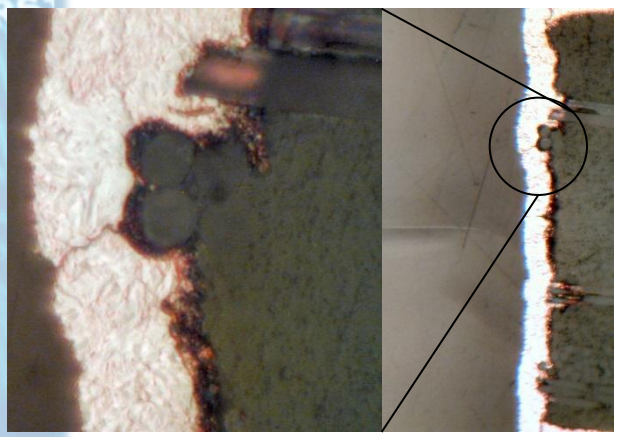
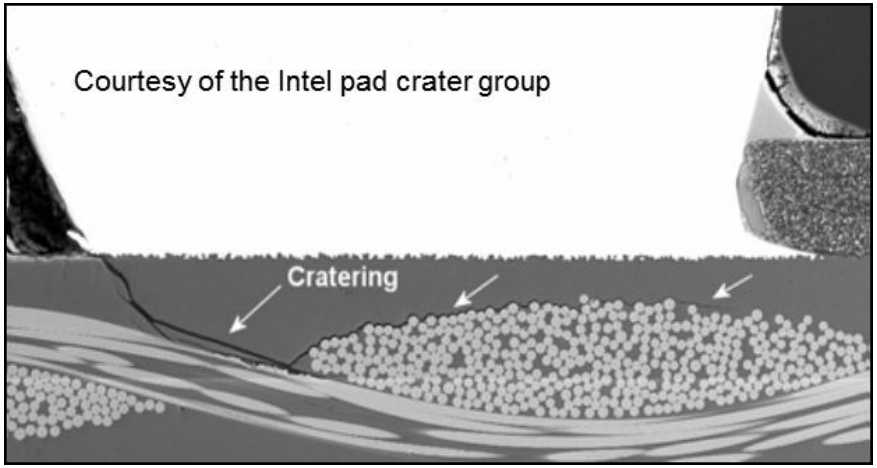


Photo4 CAF filament presence with first sanding direction

CAF Failure



Thru Hole Plating Failure



Pad Cratering

These issues are more acute at higher peak reflow temperatures

Pb-Free Board Materials Reliability

Goal

Assess the impact of the Pb-Free soldering process on latest generation of PWB laminates.

- Focus on suitability for high layer count / high thermal mass board design applications in which board surface could see temperatures up to 260° C peak reflow temperature.
- Fine tune the testing process between consecutive phases
- Select recently launched or about to be launched materials

Project History

- 56 materials tested to date. More planned.
  - Phase1 completed 2008 – 23 laminates
  - Phase 2 completed 2011 – 20 laminates
  - Phase 3 completed Q1 2014– 13 laminates
  - Phase 4 commenced 2013 – 12 laminates

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Overview

- 12 laminate/pre-preg materials to be evaluated
- MRT-5 TV, 20 layer construction, 2 different resin contents.
  - Standard Resin
    - Laminate - 1 sheet 2116 glass cloth - 53% resin content.
    - Pre-preg – 1 sheet 1080 glass cloth – 62% resin content.
  - High Resin
    - Laminate - 2 sheets 106 glass cloth - 71% resin content.
    - Pre-preg – 1 sheet 1080 glass cloth – 67% resin content
- 6 x SMT reflow cycles preconditioning at 260°C peak (50% of samples)
- Test plan same as phases 2 and 3

Why 260°C and why 6 Cycles?

Why 260°C?

- Our OEM members needed to know the impact of Pb-free reflow on complex, high reliability infrastructure products (currently ROHS exempt but transitioning to PB Free shortly).
- These products typically are thick multi-layer with densely packed components including large ceramic devices.
- Achieving sufficient reflow temperatures (235°C) at the higher thermal mass components results in areas of the board seeing temperatures up to 260°C

Why 6 cycles?

- These boards typically are double sided SMT, often with additional wave soldering requirements. Furthermore, they are very expensive and therefore the ability to replace defective components is vital. 6 reflow cycles simulates a worst case scenario that a board of this type is likely to see.

Project Benefits

For the OEM:

- A direct comparison of the performance of a large range of laminates allowing designers to select (or shortlist) the best materials for specific product requirements.
- Unique test data on how materials perform under higher SMT reflow temperatures (260°C peak) typically needed for high layer, densely populated, high reliability products.
- Independent testing specified by HDP OEM members and appropriate to current product qualification demands.

For the material contributor:

- An opportunity to showcase materials and demonstrate how they perform against other suppliers' materials.
- Extensive independent test data that can be used to enhance in house qualification data.
- A chance to rank laminate performance against competition for each type of test performed and identify product strengths and weaknesses

Final Material List

FR4

- Shengyi S1000-2M

Semi-Hi Speed

- TUC TU865

Tier II Hi-Speed

- Hitachi MCL-HE-679G(S)
- Nanya NP-170D
- EMC EM-888

Tier III Hi-Speed

- TUC TU-883
- Shengyi S7439
- ITEQ IT-968
- EMC EM-891

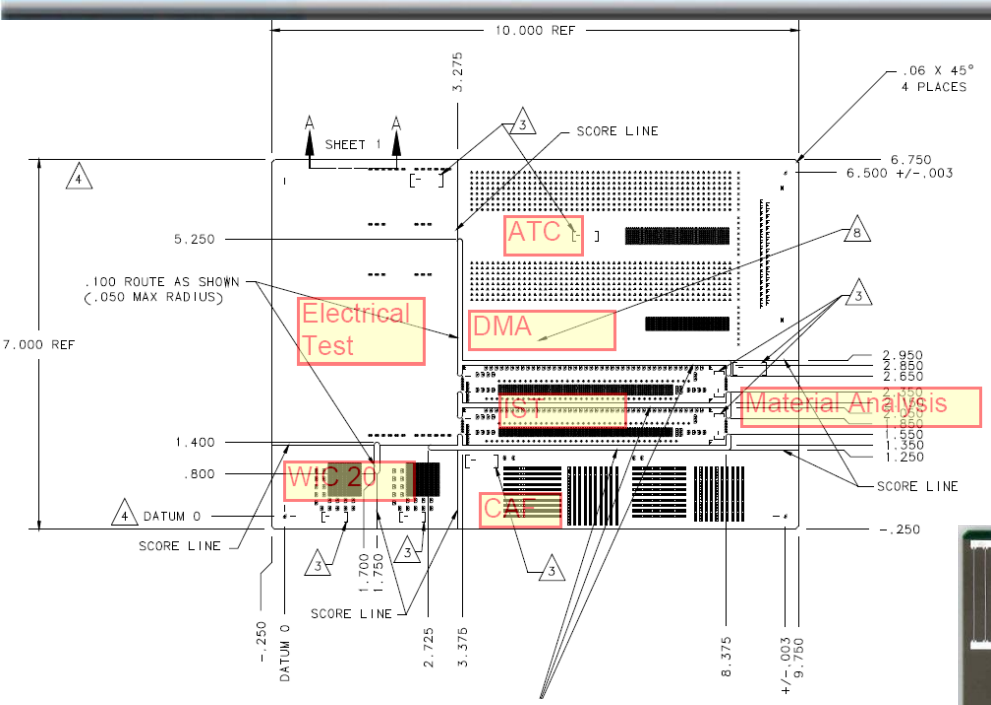
Tier IV Hi-Speed

- Panasonic Meg7
- TUC TU-933
- Hitachi LW-990G

Several materials selected that are not expected to have UL approval until early 2014.

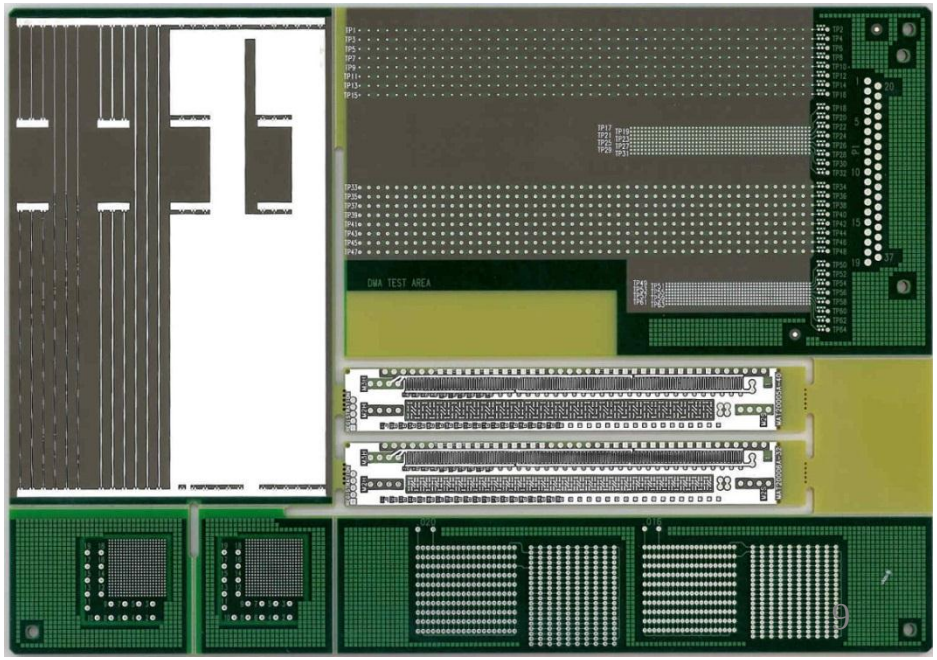
Viasystems will work with each material supplier to optimize board fabrication processes.

Test Vehicle Sections



Through hole via pitches – 1.0mm and 0.8mm

7 sections on Test Vehicle



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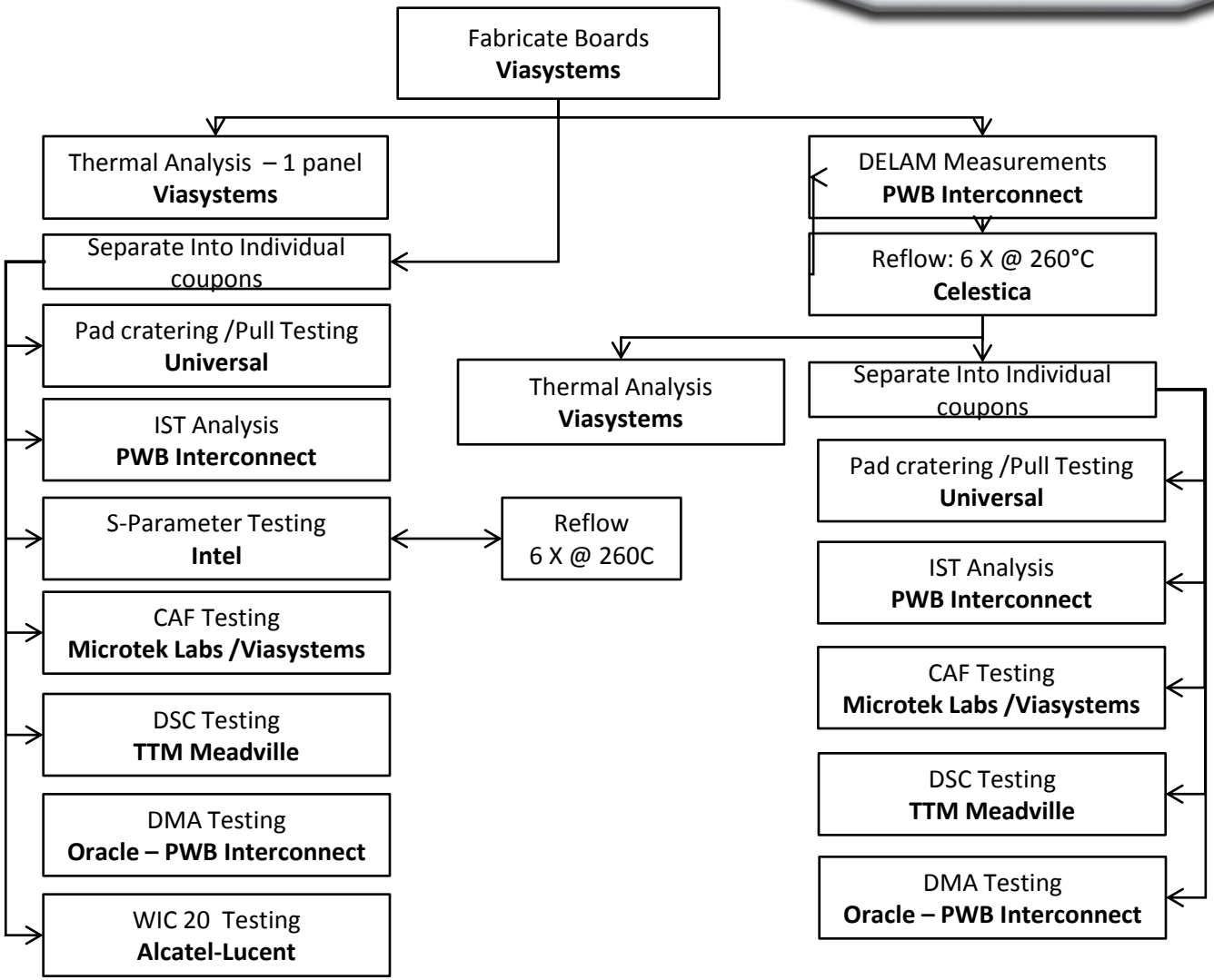
Pb-Free PWB Materials Reliability Test Program



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Project Schedule

Project Task	Plan
Test Board Fabrication	15-Jul-14
Pre-Conditioning / DELAM testing	13-Oct-14
WIC 20 testing	13-Oct-14
S-Parameter testing	27-Oct-14
Thermal Stress Testing	18-Nov-14
Pad Pull Testing	18-Nov-14
CAF testing (CAF Coupons)	25-Jan-15
CAF testing (IST Coupons)	1-Feb-15
Thermal Anaysis	1-Feb-15
IST testing	3-Mar-15
Final Report	2-Apr-15

Project Participants

- Alcatel-Lucent
- Celestica
- Ciena
- Curtiss Wright
- EMC
- Hitachi
- IBM
- Intel
- Isola
- ITEQ
- Multek
- Oracle
- Panasonic
- PWB Interconnect
- Shengyi
- TTM Meadville
- TUC
- Viasystems

Impact of PWB Design on Pb-Free SMT Reflow Induced Material Damage

Project Leader : John Wilson, IBM
Project Facilitator : Brian Smith, HDP User Group

26th February 2014

Background for Project

- In our 3 previous Pb-free materials reliability projects, we have found that the pitch of through hole vias plays a major role in the Pb-free assembly survivability of a material → 0.8mm significantly worse than 1.0mm pitch.
- We also know from previous testing (ALU and others) that board thickness/layer count/resin content (all of these affect the Z-axis expansion of the boards) are also key variables in the Pb-free assembly survivability.
- There has also been some limited data that suggests more plane layers in the center of the board adversely affects material survivability. (Some of this may be related to Cu weight also.)

Capacitance through Reflow

IST Coupons Exhibiting Material Degradation (Delamination) Following 6X 260°C Reflow Cycles					
Assembly Level	Reflow Cycle #2 (Out of 5)	Reflow Cycle # 3 (Out of 5)	Reflow Cycle #4 (Out of 5)	Reflow Cycle #6 (Out of 8)	Reflow Cycle #6 Only
	Minimum	Standard	One Rework	BGA Rework	BGA Rework
Material Dash #	.032" / 0.8mm Coupons				.040" / 1mm
71	0	0	0	0	No
72	0	0	0	0	No
73	0	0	0	0	No
74	0	0	0	0	No
75	0	40%	80%	88%	No
76	0	80%	80%	100%	No
77	0	20%	40%	100%	No
78	0	0	60%	100%	Yes
79	0	0	0	0	No
80	0	0	20%	100%	No
81	100%	100%	100%	100%	Yes
82	100%	100%	100%	100%	Yes
83	0	40%	40%	50%	No
84	0	20%	80%	100%	No
85	0	0	0	0	No
86	0	0	0	0	No
87	0	0	0	100%	No
88	0	20%	100%	100%	Yes
89	0	60%	100%	100%	No
90	100%	100%	100%	100%	Yes
93	0	0	0	65%	No
94	0	0	0	88%	No
95	0	0	0	0	No
96	0	0	0	0	No

Testing conducted by PWB Interconnect Solutions using Dielectric Estimation Laminate Assessment Method (DELAM)

- 15 out of 24 material cells exhibit damage on 0.032”/0.8 mm coupon
- 5 out of 24 material cells exhibit damage on 0.040”/1 mm coupon
- Capacitance results correlate with cross-section analysis.
- Capacitance measurement is a valuable tool to detect internal damage
  - 3 cells w visual damage
  - 15 cells w capacitance change
- Visual inspection alone is unreliable to detect damage.

Project Goals

- Provide data quantifying the effect of via pitch on Pb-free survivability
- Provide quantitative data on the effect of thickness/layers/resin content to a “lower complexity” based on materials that have already shown limitations in more complex constructions.
- Evaluate the effect of more central plane layers in the design.
- Further evaluate the specific materials to identify their limits.
- Provide additional data to IPC and material suppliers to better drive requirements for material evaluation and test.

Project Goal and Scope

Goal

Quantify the impact of board design on the survivability (resistance to delamination) of PWBs through the Pb-Free SMT process.

Scope

- Focus on ‘hot reflow’ cycles. 260°C peak temperatures.
- Evaluate selected materials that exhibited some delamination in phase 3 of PWB materials reliability project.
- Use a modified version of the MRT-5 test vehicle as used in PWB materials reliability project.

Project Details

- Quantify the effect of pitch
  - Add 0.9, 0.7, and 0.65mm pitch IST coupons in the place of the current S-parameter section.
  - ATC section rotated and truncated – for cross-sections and material analysis only (TMA, DMA, DSC, etc.)
  - Primary Focus on the DELAM testing

Quantify the effect of central plane layers

- Two “special” IST coupon designs (1mm or 0.8mm pitch) where more plane layers are added central to the design (4, and 6 planes rather than just 2 in current design)

Project Details

Quantify the effect of thickness/layers in conjunction with pitch

- Build 12 and 16 layer versions (previously described) and the 20 layer 58% Resin content construction (repeat build)
- Use materials we already have data on at 20 layer constructions (that passed at 1mm pitch, failed at 0.8 mm pitch)

Test Vehicle Constructions

We have a large amount of data associated with the MRT test vehicle and any testing beyond this should use this as the starting point/baseline.

- Testing to date on two 20 layer constructions (.116-.118” thick, 58% and 69% resin content)
- MRT test vehicle designed to also support a 12 layer, .093” thick, 50% resin content construction (remove layers 6-9 and 12-15)
- Design can also support a 16 layer construction (remove layers 8,9,12 and 13) – target .105” thick, 54%

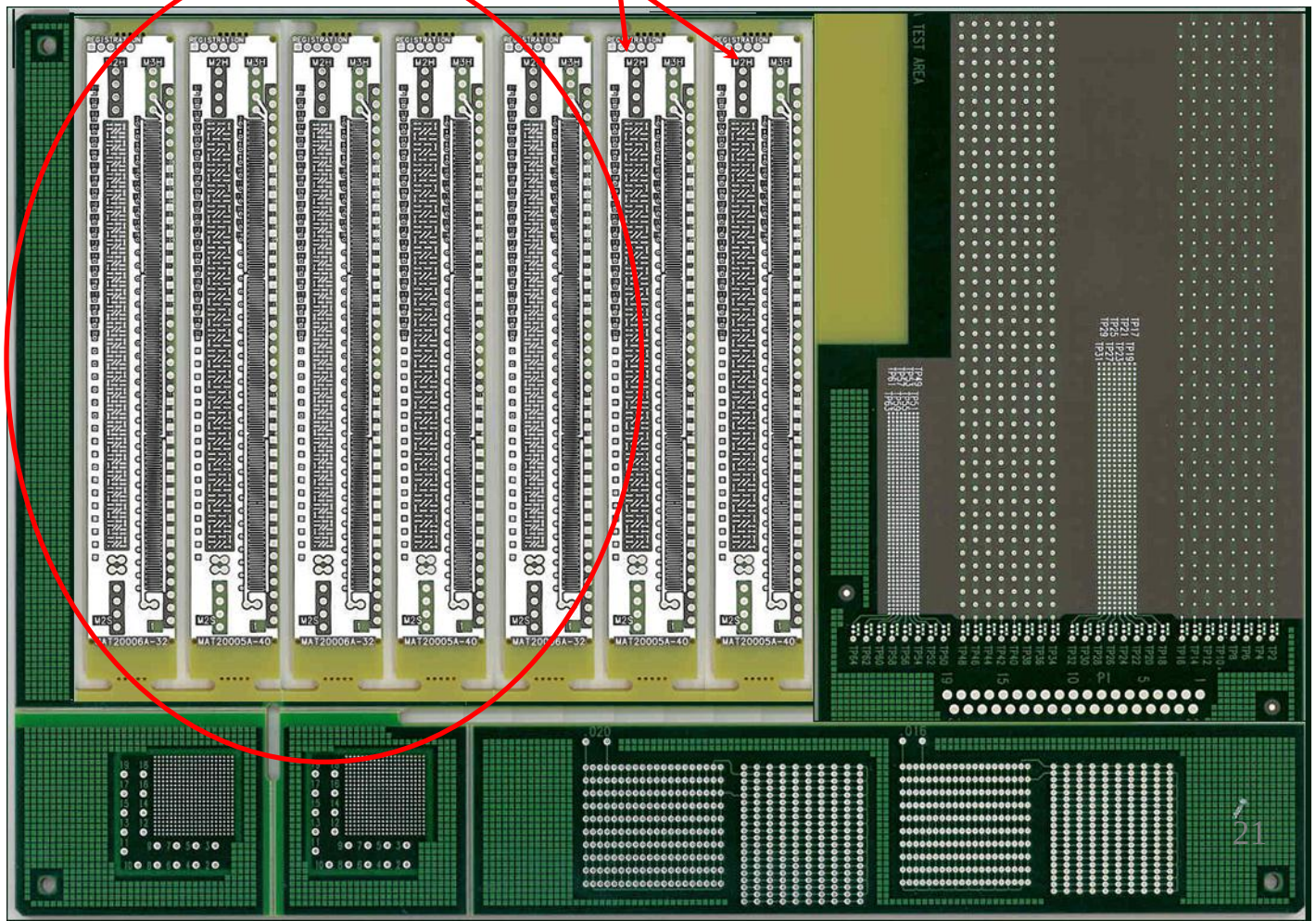
This approach ensures we are comparing material constructions, not test vehicle designs.

Modified MRT-5 for Part 1 - Proposed

Add 5 additional IST coupons

Original 2 IST coupons

ATC section rotated and truncated (for material test data and crossections)



Part 1 Proposed Materials

- Proposed materials are: ITEQ IT-180i , Shengyi S7038 , TU-872SLK
  - Materials selected as they exhibited sensitivity to via pitch and resin content during testing.
  - Total of 9 builds 12,16, 20 layer for each of 3 materials.
  - 10 test boards per build.

- Can also evaluate WIC-20, CAF, Material properties depending on project interest/support.
  - Primary focus of this is Pb-free survivability testing

Project Resources

- Design new IST Coupons (PWB Interconnect Solutions)
- Finalize material selection (Team)
- Finalize 16 layer stack up (ALU)
- Modify working artwork– placing in new IST coupons – at CAM (PWB Interconnect / Alcatel-Lucent)
- Provide materials (Shengyi, ITEQ, TUC)
- Build Modified MRT-5 Test Boards **(TBD)**
- 6X Reflow Assembly (Celestica)
- Delam (PWB Interconnect Solutions)
- WIC-20,(TBC)
- CAF Testing (If required) – PWB Interconnect